NON-ISOLATED HIGH-VOLTAGE GAIN DC–DC CONVERTERS BASED ON 3SSC AND VMC

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***Abstract*—This paper introduces a new family of DC–DC converters based on the Three-State switching cell and voltage multiplier cells. In order to verify the operating principle, the boost converter is chosen and investigated in detail. The behavior of the converter is analyzed through an extensive theoretical analysis. A closed loop circuit of DC– DC converters based on the Three-States witching cell and voltage multiplier cells is introduced in this paper using PI controller. Zieglerand Nicholstuning method is used to tune the PI controller .Equations are developed, modeled and simulated along with common power electric components utilizing MATLAB/Simlink, Sim Power System toolbox. The required output voltage is obtained by varying the reference set voltage. The setting time of the output is reduced to 0.02 sec due to the efficient operation of the PI controller**

***Key words*—Simulink, High voltage gain DC-DC converter, Static switching cell, Voltage multiplier cell.**

I. INTRODUCTION

Depending on the application nature, several types of static power converters are necessary for the adequate conversion and conditioning of the energy provided by primary sources such as photovoltaic arrays, wind turbines, and fuel cells. Besides, considering that the overall cost of renewable energy systems is high, the use of high-efficiency power electronic converters is a must. Due to the importance of the conventional boost converter in obtaining distinct and improved topologies for voltage step-up applications, some techniques have been developed and modified with the aim of improving the characteristics of the original structure. Basically, two strategies are adopted for this purpose: voltage step-up with and without using extreme values of duty cycle. Cascading one or more boost converters may be considered to obtain high voltage gain. Even though more than one power processing stage exists, the operation in continuous conduction mode (CCM) may still lead to high efficiency. The main draw backs in this case are increased complexity and the need for two sets that include active switches, magnetic, and controllers. Besides, the controllers must be synchronized and stability is of great concern. Due to high power levels and high output voltage, the latter cascaded boost stage has severe reverse losses, with consequent low efficiency and high electromagnetic interference (EMI) levels [1-2]. The efficiency of the conventional fly back structure is typically low due to the parasitic inductance. A possible solution lies in connecting the output of the boost converter to that of the fly back topology, with consequent increase of voltage gain due to the existent coupling between the arrangements. In this case, the boost convert behaves as an active clamping circuit when the main switch of the fly back stage is turned OFF. This project presents the topology for voltage step-up applications based on the use of multiplier cells constituted by diodes and capacitors. The converter is able to operate in overlapping mode (when a duty cycle D is higher than0.5) and non over lapping mode (when a duty cycle D is lower than 0.5), analogously to other 3SSC-based structures. However, the study carried out in this paper only considers the operation with D>0.5[3-4]. The generic structure, which is valid for any number of cells, is initially presented, while the analysis is focused on structures with three cells, aiming to determine the stress regarding the elements that constitute the afore mentioned configurations. Experimental results regarding the structure with three multiplier cells are also presented and discussed to validate the proposal. For good operation of the VMC ac input voltage is required, which is an important requirement of this cell. Due to this fact, the use of the 3SSC depicted is considered because it generates such ac voltage across the terminals of the autotransformer and the drain terminals of the controlled switches. For this reason, both cells are integrated leading to the proposed cell In the resulting cell, the controlled switches can be represented by MOSFETs, junction field-effect transistors, insulated gate bipolar transistors, bipolar junction transistors, etc. All the generated topologies present bidirectional characteristics. By using the proposed cell, it is possible to generate the six novel non isolated dc–dc converters, i.e., buck, boost, buck–boost, Cuk, SEPIC, and zeta. As was mentioned before, the use of high- voltage gain converters is of great interest, even though many approaches are based on isolated topologies [5-8]. It is worth to notice that the use of non isolated converters particularly dedicated to applications regarding renewable power systems has been the scope of recent works [9-10] The efforts leading to the development of such non isolated topologies are then well justified in the literature [11].In order to verify the claimed advantages of the converter family, the boost converter is chosen. The developed analysis considers the converter associated with three voltage multiplier cells and is detailed as follows. In order to better understand the operating principle of then structures, the following assumptions are made:

1) The input voltage is lower than the output voltage;
2) Steady-state operation is considered;
3) Semiconductors and magnetic are ideals;

4) Switching frequency is constant;
5) The turn's ratio of the autotransformer is unity;
6) The drive signals applied to the switches are 180◦displaced.

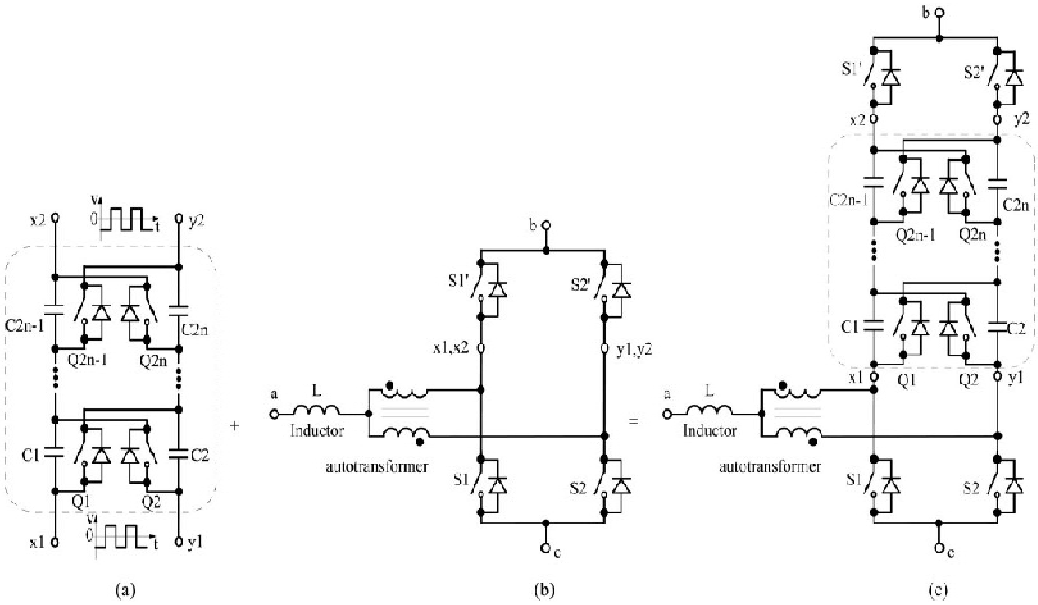

Figure.1.Circuit diagram

(a) 3 State Switching Cell (b) Voltage Multiplier Cell (c) Resulting Circuit

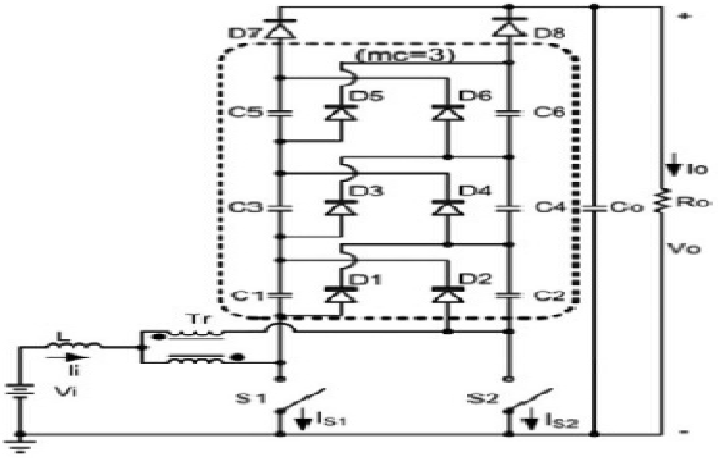

Figure2.Proposed Boost converter using three VMCs

II. OPERATING PRINCIPLE

The configuration that uses three multiplier cells is represented in figure2. The equivalent circuits that correspond to the converter operation and there theoretical wave forms are presented in figure3.

A. First stage [t0,t1] [Figure3 (a)]

Switches *S*1and *S*2are turned ON, while all diodes are reverse biased. Energy is stored in inductor *L* and there is no energy transfer to the load. The output capacitor provides energy to the load. This stage finishes when switch *S*1 is turned OFF.

B. Second stage [t1,t2] [Figure3(b)]

Switch *S*1 is turned OFF, while *S*2 is still turned ON and diode *D*5 is forward biased. There is no energy transfer to the load as well. Inductor *L* stores energy, capacitors *C*1 and *C*3 are discharged, and capacitors *C*2, C4, and *C*6 are charged.

C. Third stage [t2,t3] [Figure3(c)]

Switches *S*1 and *S*2 remain turned OFF and ON, respectively. Diodes *D*3 and *D*7are forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through *D*7.The inductor stores energy and capacitors *C*2 and *C*4ares till charged. Capacitors *C*1 are discharged and so are*C*3 and*C*5.

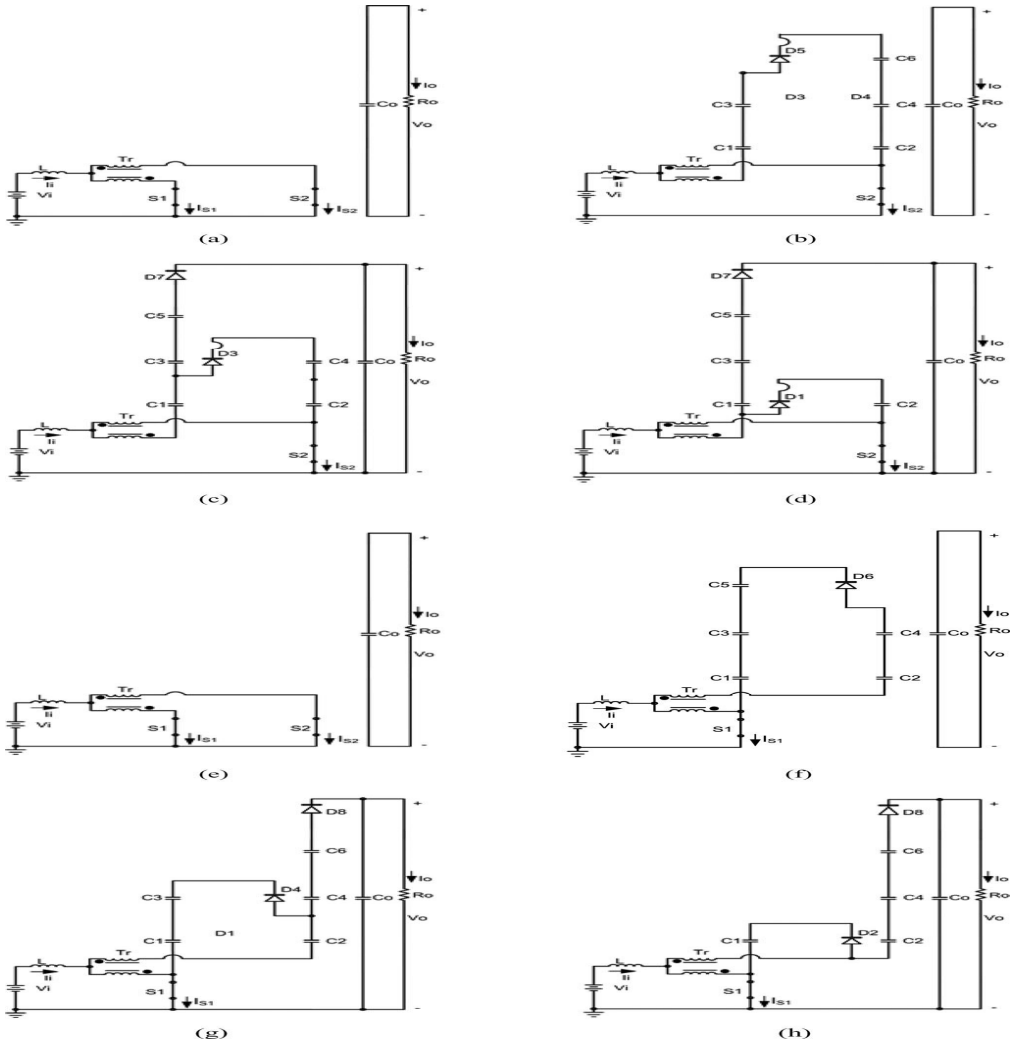

Figure.3.Operatingstages:(a)first stage,(b)second stage,(c)third stage,(d) fourth stage,(e)fifth stage, (f)sixth stage,(g)seventh stage, and(h)eighth stage.

D. **Fourth stage [t_3,t_4] [Figure3(d)]**

Switch *S*2 remains turned ON, diode *D*3 is reverse biased, and diode *D*1 is forward biased. Energy is transferred to the load through *D*7.The inductor is discharged, and so are capacitors *C*1, C3, and*C*5, while *C*2 is charged.

E. **Fifth stage [t4,t5] [Figure3(e)]**

This stage is identical to the first one.

F. **Sixth stage[t5,t6] [Figure3(f)]**

Switch *S*2 is turned OFF and switch *S*1 is still turned ON. Diode *D*6 is forward biased. The inductor is charged by the input source, although capacitors *C*2 and *C*4 are discharged instead.

G. **Seventh stage [t6,t7][Figure3(g)]**

This stage is similar to the third one.

H. **Eighth stage [t7,t8] [Figure3 (h)]**

Switch *S*1is turned ON, while *S*2 remains turned OFF. Diodes *D*2 and *D*8 are forward biased, while *D*4is reverse biased as well as the remaining diodes. Energy transfer to the load occurs through *D*8, and capacitor *Co is* still charged. The inductor is discharged, while capacitor *C*1is charged and capacitors*C*2, *C*4, and*C*6 are discharged.

Static Gain

The static gain for the generic structure of the boost converter can be obtained from the inductor volt–second balance. The voltage area multiplied by the time interval that corresponds to the inductor charge is equal to that regarding the inductor discharged. T he following expression can then be derived:

$$G_v = \frac{V_o}{V_i} = \frac{(mc+1)}{(1-D)} \qquad (1)$$

Where, *mc* is the number of voltage multiplier cells; $V_i$is the input voltage; V_o is the output voltage; and *D* is the duty cycle. Expression (1)is plotted and shown infigure4, where one can see that the static gain changes when $D<0.5$, as represented by the dotted line .It occurs because the multiplier capacitors are not fully charged due to the reduced charge time.

III DESIGN PROCEDURE

A. Preliminary Calculation

The maximum input power is in (2)

$$P_i = \frac{P_o}{\eta} = 1052.3\ \text{W}. \tag{2}$$

The maximum duty cycle is obtained using (3) as follows:

$$D_{\max} = \frac{V_o - V_{i(\min)} \cdot (mc+1)}{V_o} = 0.58. \tag{3}$$

The average and maximum values o f the input current are given by (4) and (5), respectively

$$I_{L(\text{avg})} = I_{i(\text{avg})} = \frac{P_o}{V_{i(\min)} \cdot \eta} = 25.06\ \text{A} \tag{4}$$

$$I_{L(\max)} = \frac{P_o}{V_{i(\min)} \cdot \eta} + \frac{\Delta I_L}{2} = 26.94\ \text{A}. \tag{5}$$

Besides, the normalized ripple current β as a function of the duty cycle is given by

$$\beta = \frac{2 \cdot L \cdot \Delta I_L \cdot f_s}{V_o} = \frac{(1-D) \cdot (2D-1)}{(mc+1)}. \tag{6}$$

Expression (6) is plotted in figure5, where it can be seen that for curve *mc=3* and duty cycle *D*=0.75the maximum normalized ripple current is β=0.03125. Therespective inductanceis calculatedfrom (7)as

$$L = \frac{V_o \cdot \beta}{2 \cdot f_s \cdot \Delta I_L} \cong 70\ \mu\text{H}. \tag{7}$$

The core loss in the inductor is given in (8)

$$P_{L(\text{core})} = \Delta B^{2.4} \cdot \left(K_H \cdot f_L + K_E \cdot f_L^2\right) \cdot V_e = 0.075\ \text{W} \tag{8}$$

Where ,ΔB= 0.045T is the magnetic flux variation; $KH=4\times10^{-5}$ is the hysteresis loss coefficient; f_L =2,f_s =50 kHz is the operating frequency of the inductor; $KE=4\times10^{-10}$ is the eddy-current loss coefficient; and V_e=42.50cm^3 is the volume of Thornton coreNEE-55/28/21.

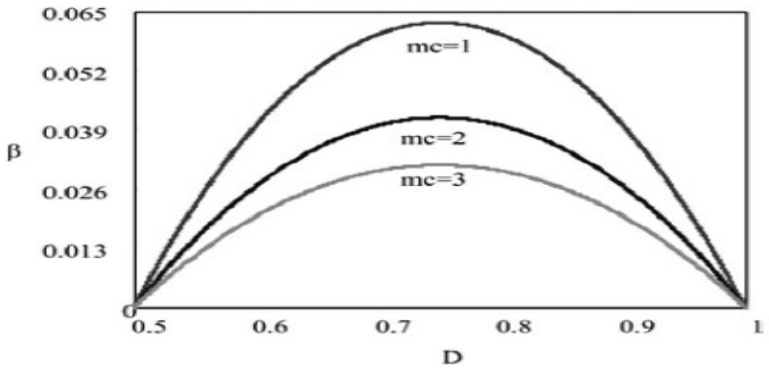

Figure.4. Normalized ripple current as a function of the duty cycle.

The copper loss in the inductor is

$$P_{L(\text{copper})} = \frac{\rho \cdot l_t \cdot N_L \cdot I_{L(\text{rms})}^2}{n_L \cdot S_f} = 2.89\ \text{W} \tag{9}$$

Where, ρ =2.078×10^{-6} Ω·cm is the copper resistivity at70◦C; l_t =11.6cm is the average length of one turn; N_L = 15 is the number of turns of the inductor; $I_{L(\text{rms})}$ =25.06A is the rms current through the inductor ;n_L = 62 is the number of wires in parallel ;S_f=0.001287cm^2 is the cross-sectional area of copperwireAWG26.

B. Autotransformer

The active power processed by the high-frequency autotransformer is obtained similarly to that processed by its low frequency counterpart, as demonstrated in [7]. Besides, it has been shown that it corresponds to half of the total output power. The design procedure of such a magnetic element is analogous to that for the transformer of a conventional full-bridge converter [8], i.e.

$$A_e A_w = \frac{P_t/2}{K_T \cdot K_U \cdot K_P \cdot J_{\max} \cdot \Delta B_{\max} \cdot 2 \cdot f_s} \cdot 10^4 = 12.22\,\text{cm}^4 \qquad C_o \cong \frac{I_o \cdot (2D_{\max} - 1)}{\Delta V_{Co} \cdot 2 \cdot f_s} \cong 2\,\mu\text{F} \tag{10}$$

Where, *Ae*, *Aw* is the core area product; K_T =1isthe topology factor; K_U=0.4 is the window utilization factor; K_P= 0.41 is the primary winding utilization factor

Table.1 Design Specifications

Parameter	Specification
Rated output power	P_o=1000 W
Minimum input voltage	$V_{i(min)}$=42 V
Maximum input voltage	$V_{i(max)}$=54 V
Rated input voltage	V_i=48 V
Output voltage	V_o=400 V
Number of multiplier cells	mc=3
Switching frequency	f_s=25 kHz
Maximum ripple current through inductor L	ΔI_L=15%·$I_{L(avg)}$
Ripple voltage through multiplier capacitors $C_1 \ldots C_6$	ΔV_{Ck}=8.75%·V_o
Ripple voltage through output capacitor C_o	ΔV_{Co}=1%·V_o
Expected theoretical efficiency	η=95%
Autotransformer turns ratio	a=1

$J_{\max}$ = 350 A/cm^2 is the magnetic flux density; $\Delta B_{\max}$ =0.15 is the maximum magnetic flux variation; and fs =25 kHz is the operating frequency of the transformer. CoreNEE-65/33/26 manufactured by Thornton is then chosen, whose characteristics are as follows: A_e =5.32cm^2 is the effective core cross-sectional area; A_w =3.7cm^2 is the window area considering the former coil; A_eA_w =19.68cm^4; and V_E =78.2 cm^3 is the core volume. The number of turns for the autotransformer windings is

$$N_T = \frac{V_{i\min}}{2 \cdot (1 - D_{\max}) \cdot A_e \cdot \Delta B_{\max} \cdot 2 \cdot f_s} \cdot 10^4 \geq 12.53\,\text{turns.} \tag{11}$$

Considering the presence of the skin effect, the maximum diameter of the conductor used in the windings must be lower than [6].

$$d_f = 2 \cdot \frac{6.62}{\sqrt{f_s}} = 2 \cdot \frac{6.62}{\sqrt{25 \times 10^3}} = 0.084\,\text{cm.} \tag{12}$$

The core loss in the autotransformer is given by

$$P_{T(\text{core})} = \Delta B^{2.4} \cdot \left(K_H \cdot f_T + K_E \cdot f_T^2\right) \cdot V_E = 2.4714\,\text{W} \tag{13}$$

Where, ΔB=0.15is the magnetic flux variation; K_H = 4×10^{-5}is the hysteresis loss coefficient; K_E=4×10^{-10} is the eddy current loss coefficient; and V_e =78.2cm^3 is the core volume. The copper loss in the windings of the transformer is

$$P_{T(\text{copper})} = \frac{2 \cdot \rho \cdot l_T \cdot N_T \cdot I_{T(\text{rms})}^2}{n_T \cdot S_f} = 4.90\,\text{W} \tag{14}$$

Where, ρ =2.078×10^{-6}Ω·cm is the copper resistivity at70◦C; lT=14.24cm is the average length of one turn; n_T= 28 is the number of wires in parallel; S_f =0.001287cm^2 is the cross-sectional area of copper wire AWG26; and N_T =19 is the number of turns.

C. Capacitors

The multiplier capacitors C_n and the output capacitor C_o can be obtained from the following expressions:

$$C_n = C_{n+1} = \frac{(mc - n + 1)}{8} \frac{I_{i(\text{avg})} \cdot (1 - D_{\max})}{f_s \cdot \Delta V_{Ck}}$$

$$\text{for } n = 1, 2, 3, \text{ and } mc = 3$$

$$C_1 = C_2 \cong 4.5\,\mu\text{F} \quad C_3 = C_4 \cong 3.0\,\mu\text{F} \quad C_5 = C_6 \cong 1.5\,\mu\text{F} \tag{15}$$

In standalone applications, an inverter is typically connected to the output of the high-gain dc–dc converter. Considering this type of application, a 470μF/450V capacitance was adopted for the filter capacitor Co.

D. Main Switches

The maximum voltage across the main switches $S1$ and $S2$, diodes $D7$ and $D8$, and multiplier capacitors $C1 \ldots C6$ is given by (16) which is valid when the ripple voltage across the capacitors is neglected:

$$V_{S1-S2} = V_{C1-C6} = V_{D7-D8} = \frac{V_{i(\min)}}{(1 - D_{\max})} = 114.28\,\text{V}. \tag{16}$$

The average current and the rms current through the switches are given by (17) and(18), respectively

$$I_{S1(\text{avg})} = I_{S2(\text{avg})} = \frac{1}{8} \cdot (D_{\max} + 3) I_{L(\max)} = 11.21\,\text{A} \tag{17}$$

$$I_{S1(\text{rms})} = I_{S2(\text{rms})} = \frac{I_{L(\max)}}{24} \cdot \sqrt{3(101 - 53 D_{\max})} = 15.16\,\text{A}. \tag{18}$$

MOSFET IRFP 4227 is then chosen as the main switch, whose characteristics are as follows: drain to source voltage VDS=200V; diode forward voltage $V_{(F)}$ =1.3V; drain current I_D =46AatT_c =100◦C; on resistance $R_{DS\,(\text{on})}$ =37.9mΩ at T_j =100◦C; rise time TR=20ns; fall time t_f=31 ns. The conduction loss regarding each main switch is obtained from

$$P_{S1\ldots S2(\text{cond.})} = R_{DS(\text{on})} \cdot I^2_{S1(\text{rms})} = 8.71\,\text{W}. \tag{19}$$

The switching loss during turn ON and turn OFF for a single switch is

$$P_{S1\ldots S2(\text{sw.})} = \frac{f_s}{2} \cdot (t_r + t_f) \cdot I_{S1(\text{avg})} \cdot V_{S1} = 0.837\,\text{W}.$$

IV. CLOSED LOOP DESIGN

Design of PI controller using Ziegler-Nichols Tuning

1. First, note whether the required proportional control gain is positive or negative. To do so, step the input up (increased) a little, under manual control, to see if the resulting steady state value of the process output has also moved up (increased). If so, then the steady-state process gain is positive and the required Proportional control
2. Turn the controller to P-only mode, i.e .turn both the Integral and Derivative modes off
3. Turn the controller gain, *Kc* ,up slowly (more positive if *Kc* was decided to be so instep1 ,otherwise more negative if *Kc* was found to be negative in step1) and observe the output response. Note that this requires changing *Kc* instep increments and waiting for a steady state in the output, before another change in *Kc* is implemented
4. When a value of *Kc* results in a sustained periodic oscillation in the output (or close to it), mark this critical value of *Kc* as *Ku*, the ultimate gain. Also, measure the period of oscillation, Pu, referred to as the ultimate period .(Hint: for the system A in the PID simulator, *Ku* should bearound0.7 and 0.8 .Using the values of the ultimate gain, *Ku*, and the ultimate period, *Pu*, Zieglerand Nichols(Table 5) prescribe the following values for *Kc*, *tI* and *tD*, depending on which type of controller is desired.

Table- 1 Ziegler-Nichols Tuning Chart

	K_c	t_I	t_D
P control	$K_u/2$		
PI control	$K_u/2.2$	$P_u/1.2$	
PID control	$K_u/1.7$	$P_u/2$	$P_u/8$

V. SIMULATION RESULTS

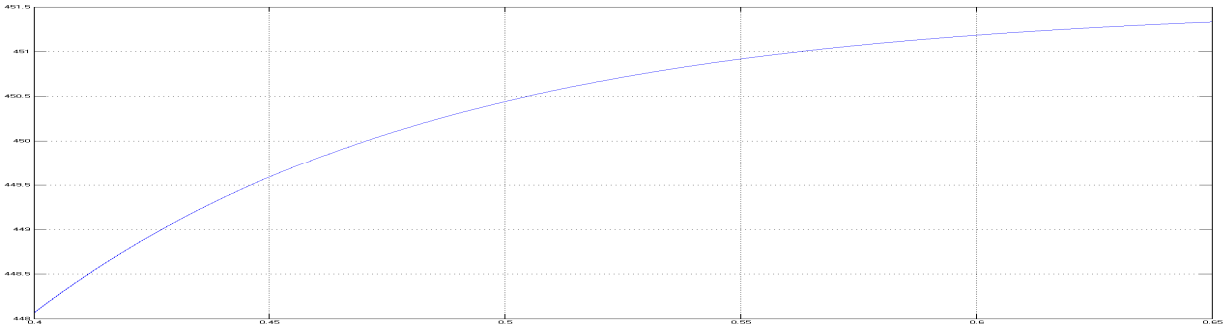

Figure.5. Open loop operation of proposed converter

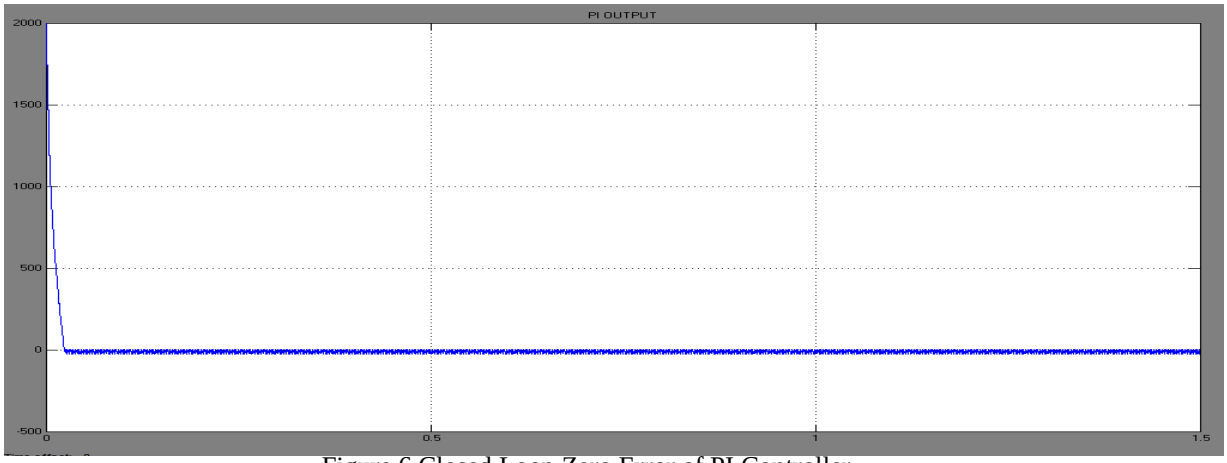

Figure.6.Closed Loop Zero Error of PI Controller

Fig. 4 shows the open loop operation of DC-DC converter in which input 9.4 V is boosted to 400 V, but the setting time is high due to open loop. Fig.5 shows the close loop zero error for PI controller to improve the performance of the controller. Fig.6 shows the switching pulse waveform to trigger the MOSFET devices. Fig 7 shows the proposed output for closed loop system. Here 9.4V is boosted to 400V by and the setting time is very less compared to open loop operation. Thus shows the effectiveness of the system.

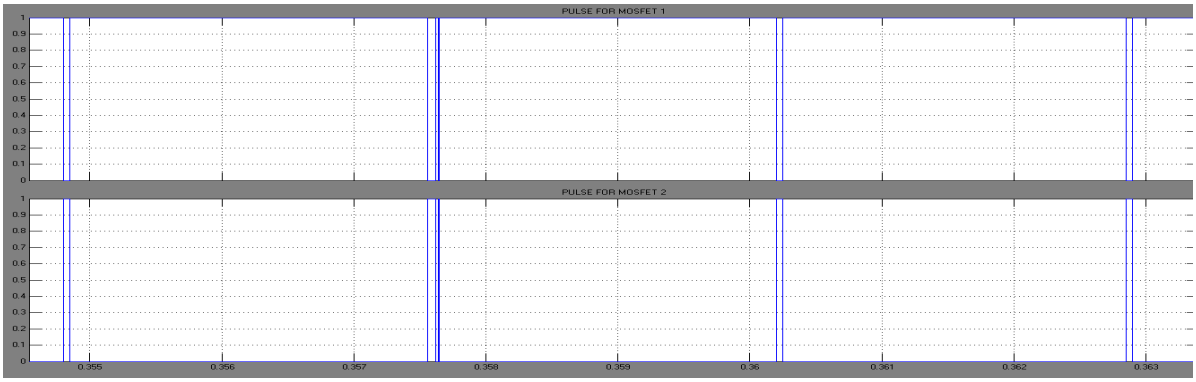

Figure.7.Switching Pulse Waveform

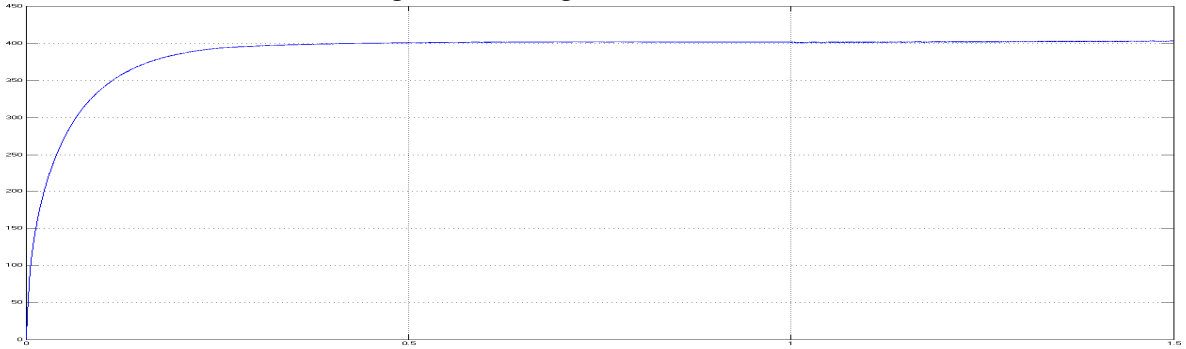

Figure.8. Closed Loop Output

VI. CONCLUSION

Thus a closed loop circuit of DC– DC converters based on the Three-States witching cell and voltage multiplier cells was introduced in this paper using PI controller. Zieglerand Nichols tuning method is used to tune the PI controller .Equations are developed, modeled and simulated along with common power electric components utilizing MATLAB/Simlink, Sim Power System toolbox. The required output voltage is obtained by varying the reference set voltage. The setting time of the output is reduced to 0.02 sec due to the efficient operation of the PI controller.

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