New Ultra Small Satellite Image Capturing Subsystem Development For Leo Application

Chafaa Hamrouni, Bilel Neji, Mohamed ben Amor, Hiroshi Nakajima, Adel M. Alimi

Abstract: Ultra small scale satellites have a very demanding and limited mass and power budget specification; therefore, mostly the design constraints prevent the use of small scale camera. In this paper, an imaging capturing subsystem is proposed for ultra small satellite, which includes low power consumption components; the developed imaging capturing subsystem was studied, simulated and successfully integrated in order to operate on board Femto satellite and cooperate with ERPSat-1 pico satellite during mission in Leo. In addition, the simulation has shown results that motivate integration of ultra small satellite with cubic sat during mission for space observation.

Index Terms: Analog Digital Converter(ADC), Color-Filter Array(CFA), Complementary Metal Oxide Semiconductor(CMOS), Charge Coupled Devices(CCD).

1 INTRODUCTION

Asignificant amount of breakthrough achievements in both science and technology in areas such as electronics, telecommunications and materials for the last decade have provoked a dramatically change in the modern understanding of a spacecraft as a technical system. A tendency to decrease mass, volume and power consumption of a spacecraft in space market areas such as Earth observation, remote sensing and scientific in general has led to the rapid development of a generation of micro, nano, pico and Femto-satellites. Imaging capability on Femto-Satellite opens the horizon for new possibilities for future small satellites' missions [1]. Some of these capabilities have already been explored by university satellites producers. Since small scale satellite have very demanding and limited mass, power and transmitted budget specification therefore, mostly the design constraints prevent the use of small scale camera. Therefore, a miniaturized camera to support these basic and developed applications needs to be developed. Requirement of these applications are very demanding and interrelated with Femto-Satellite mission.

- Chafaa Hamrouni is a PhD student, Researcher in University of Sfax, National School of Engineering of Sfax (ENIS), ReGIM Laboratory, (Tunisia) and Expert in Tecom Studies and Research Center (CERT). chafaa.hamrouni@ieee.org
- Bilel Neji is a PhD student at the University of Buffalo, N.Y, USA and Research Group on Intelligent Machines ReGIM Laboratory, (Tunisia). Bilel.neji@ieee.org
- Mohamed ben Amor is a Director in the Minisytry of Information and Communication Technologies, Tunisia. mohamed.benamor@mincom.tn
- Hiroshi Nakajima is a Professor and Director in Omron Corp., Japan. nak@ari.ncl.omron.co.jp
- Adel M. Alimi is Professor in the University of Sfax, National School of Engineering of Sfax (ENIS), and Director of the ReGIM Laboratory in Tunisia. Adel.alimi@ieee.org

Aspects of Femto size satellite missions impose the different constraint of the design of this camera. Particularly an imaging system capable of supporting these applications could provide a platform for developing further application. In this work, is presented a contribution in image capturing on board Femto-Satellite, constraints which must be respected to realize a reliable performance, specification of the imaging subsystem on board ultra small satellite and requirements, and a presentation of the contribution on study and the design of the developed sub--system: schematic design, generated layout, PCB..

2 Small Satellite Imaging Subsystem Develop.

Small satellites in the range of Femto-Satellite are the cost effective solution to investigate certain applications. Imaging systems integration on these small satellites would be helpful to realize certain application such us earth observation which consist on observing earth by capturing Images of the earth surface using various imagers. Imaging on board Femto-Satellite is specified by some requirements. To ensure the success of image capture on space several constraints which characterize the space environment must be taken into account. This chapter reviews the mass, volume and power limitations for an imaging system. It also contains the effects of electromagnetic radiation for imaging systems in small satellites.

2.1Digital Imaging System

An image sensor is a photosensitive electronic component which allows acquiring images by sensing the light (photons), thanks to its photosensitive portion (photodiode). This light energy is converted into analog voltage in the pixel and then converts a digital signal in digital, using an Analog Digital Converter (ADC). Then, the acquired image is processed to improve its characteristics (sharpness, color ...). Finally, the image is compressed in order to facilitate its transmission and storage.

2.2 Image Sensor

One of the main components of a digital imaging system is an image sensor. An image sensor is a device that converts the light from a scene that incident at its surface into an array of electrical signals. Color imaging is achieved by using a Color-Filter Array (CFA), typically green-red-green-blue Bayer CFA, which is placed on top of the image sensor pixel array. There are two possible technologies of image sensor which are Complementary Metal Oxide Semiconductor (CMOS) image

sensor [2] and Charge Coupled Devices (CCD) image sensor:

2.2.1 CMOS Image Sensor

CMOS image sensors are fabricated using standard CMOS processes with no or minor modifications [3]. Each pixel in the array is addressed through a horizontal word line and the charge or voltage signal is read out through a vertical bit line. The readout is done by transferring one row at a time to the column storage capacitors, then reading out the row using the column decoders and multiplexers. This readout method is similar to a memory structure. Figure 1 shows a typical CMOS image sensor architecture.

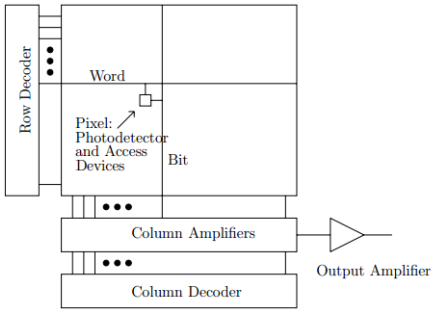

Fig. 1. Block diagram of a CMOS image sensor

2.2.2 CCD Image Sensors

CCDs have been successful in many areas of science and techniques. Their operation is close that of CMOS image sensors[4], during at information collection process, otherwise said processing of photons into electrical charges. This step is done at the photosensitive element that is the photodiode is the most important element in the pixel. However, the difference between how the two types of imaging is in the method of transportation and routing information to the pixel Analog-Digital Converters (ADCs).

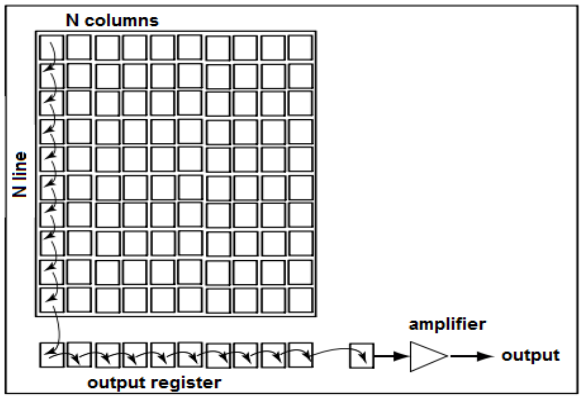

Fig. 2. Operating principle of CCD sensor

The operation of CCD is based on the charge transfer one pixel to its neighbor. This operation is based on the principle of release charges in which the photodiodes are composed of a doped silicon part of "p" type and a metal electrode.

3 Architecture Design

This chapter we will present our contribution in the design and development of the imaging subsystem of the Femto–Satellite. The components are chosen taking into account mass and size miniaturizing with the low energy consumption to meet with the imaging subsystem on board Femto-Satellite requirements [5]. Used component:

3.1 Image Sensor Selection

CMOS sensor has achieved monolithic imaging, the photoelectric imaging circuit of CMOS image sensor is integrated on a chip, this is an effective method of reducing the size and power consumption of the imaging system. With the development of manufacture technology, we have resolved the two bottle neck problem: sensor structure and sensor noise, which restricts the image quality of CMOS image sensor, and the image quality of CMOS sensor is close to or even reach the level of CCD sensor. So some CMOS image sensors are applied in certain high resolution imaging fields, especially we are all developing small satellite technology now, CMOS image sensor is ideal for space and remote sensing imaging, which requires the smaller system size, lower system power and lighter system weight, so CMOS image sensor has a very broad application prospects for our application.

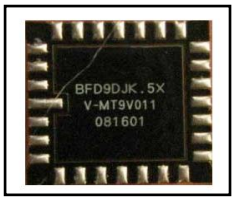

Fig. 3. MT9VO11 image sensor

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a VGA-size image at 30 frames per second (fps). An on-chip Analog-to-Digital Converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock which is synchronous with valid data.

3.2 Internal Architecture

The architecture of MT9V011 active pixel image sensor which has four main sections is shown in the figure bellow. The heart of the image sensor is an array of pixels. Within each pixel there are a photo-sensitive area and three or four transistors to buffer the photo-signal and enhance sensitivity and noise rejection. The size of the pixel array determines the spatial resolution of the image sensor. A CMOS active pixel array is randomly accessible in a similar manner to that of a Random-Access Memory (RAM). The accessibility of the pixel array is achieved via two decoders. The photo-signal is processed by an on-chip analog signal chain of circuits. There is an analog signal processor for each column. The primary function of the on- chip analog circuitry is to perform correlated double-sampling (CDS), thus to eliminate reset noise and suppressing l/f noise.

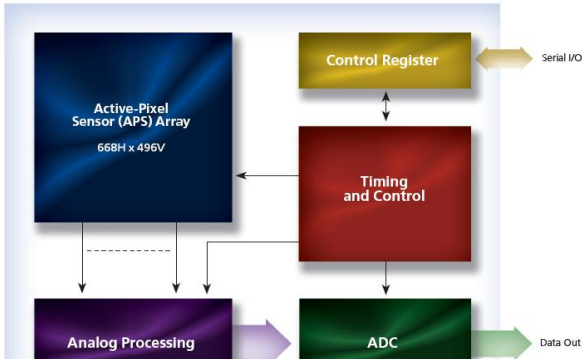

Fig. 4. MT9V011block diagram

3.3 On-Chip Timing and Control Circuitry

The clock generation as well as digital programmability circuitry can be monolithically integrated. Read-out rate, integration time, and windowing functions are to be downloaded to the chip as part of mode control in an initial set -up phase of chip operation. Once set, the chip operates in the commanded mode until further programming is received. The data output of the MT9V011 is synchronized with the PIXCLK output. When LINE_VALID is high, one 10-bit pixel datum is output every PIXCLK period.

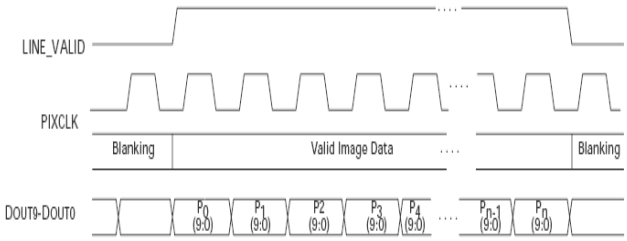

Fig. 5. Timing example of pixel data

3.4 Camera Control Processor

A camera control circuit stores an image picked up by an image sensor into an internal memory [6]. A CPU of a main processor circuit gives an instruction of reading out image data stored in the internal memory of the camera control circuit through buses and a slave access controller. After the sensor is exposed, the image data will be processed in the camera and then written to a memory card. A buffer consist of a RAM memory witch temporarily holds the image information it is written out to storage card. Image buffering is then the ability of a camera to temporarily store images in an internal memory buffer before writing them out to a memory card.

3.5 Image Signal Processor

CMOS sensors need lots of image signal processing to reproduce and enhance the quality of image. The image signal processor can help then apply real-time image enhancement, and noise reduction, and can even adjust for poor lighting conditions. The color processing blocks in the image processor are tuned to produce accurate and vivid colors in the image under a variety of lighting conditions including daylight, fluorescent and tungsten lights. To ensure the highest possible image quality, the image processing includes blocks to correct for defects and uneven responses in both the image sensor and the lens. JPEG encoder is needed to greatly reduce the quantity of binary information elements in order to represent images destined for storage or transmission. Although the images are quite varied, meaning that the information they contain may all be very different (color, light, objects), it is still preferable to put in place a unique procedure for information compression encoding, which can be applied to each image, independent of its characteristics. Typically, compressing an image consists of removing either coding redundancy or inter pixel redundancy, or both. The simplest way to compress an image is to reduce the coding redundancy using variable length-coding schemes. A variable length-coding scheme maps source symbols to a variable number of bits. Huffman coding and arithmetic coding are all well-known variable length-coding strategies. An effective way to reduce inter-pixel redundancy is to use bit-plane coding schemes. In a bit-plane coding scheme, an image is firstly decomposed into a series of binary images, and then those images are compressed by a binary compression algorithm, such as run-length coding scheme and contour-tracing and coding scheme.

4 Image Capt. Subsystem Schematic Design

The process of circuit design can cover systems ranging from complex electronic systems all the way down to the individual transistors within an integrated circuit. For simple circuits the design process can often be done by one person without needing a planned or structured design process, but for more complex designs, teams of designers following a systematic approach with intelligently guided computer simulation are becoming increasingly common. In this chapter we present the schematic design of our circuit which led to the layout generation. I used EAGLE as a software schematic designer. The schematic is developed with the EAGLE as a PCB software designer in order to generate of the layout. The next figure presents the connections between the MT9V011 CMOS image sensor and the iP2936 camera control processor. The LM317 is used as a voltage regulator to provide power supply for the image sensor, the iP2936 and for and for other components on PCB.

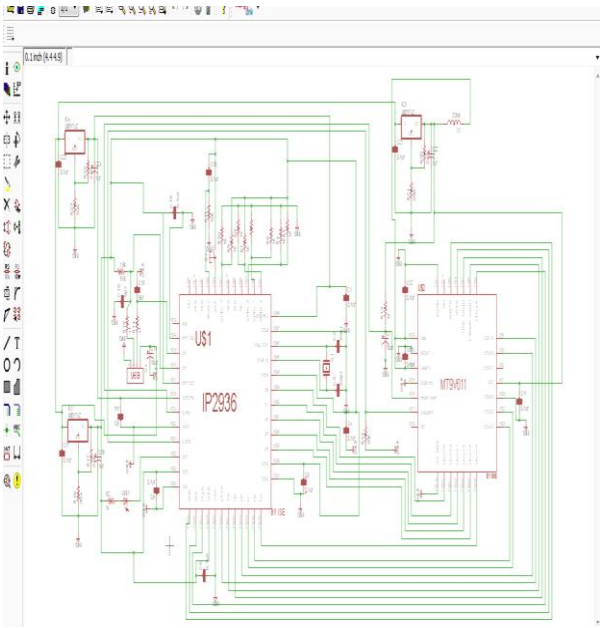

Fig. 6. System Circuit Schematic

4.1 Developed Subsystem Layout Generation

After the termination of the schematic development stage, we move to the stage of the component placement and routing to get our layout. The “switch to board” command is used then.Components placing and routing: the figure bellow represents the top and bottom board of our circuit. The blue wires present the bottom board and the red ones represent the top board The generation of the top board and the bottom board can be in separate boards. the layout generation: the layout generation is the final step. The layouts are the outcomes of the board.

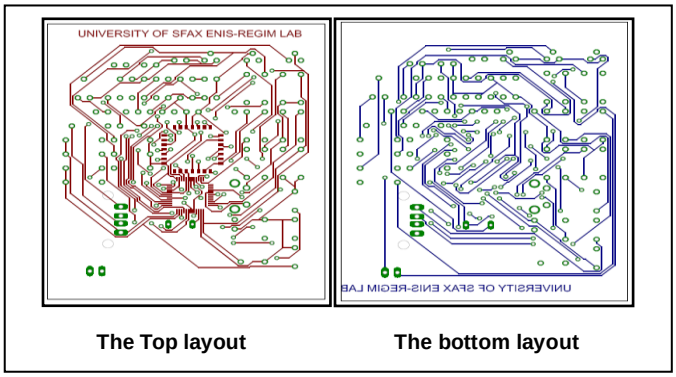

Fig. 7. The circuit schematic

The miniaturization of the circuit size is required by our application so that in this chapter we develop the layout of our electronic-card double sided.

5 Conclusion

Small camera on femto-satellite is proposed to accomplish with picosat, which wasn’t realized yet in Leo. Developed camera from the market can be purchased and be used but, designing a system provides more flexibility in term of selection of components for particular design objective and to support multiple applications. Also it provides flexibility for selection and designing particular optics for such mission. If a particular design is available, the PCB can be modified to support the optical assembly. Based on the application requirement different alternatives were proposed, since the power and the mass budget of current small satellites are very demanding to meet, we have chosen a digital camera design which combine the capture and the processing into one card to significantly reduce the system size and power consumption. For prototype, optics compatible with camera with reasonable field of view has been used. But this optics needs to be replaced with the proposed state of the art solutions.

Acknowledgment

The Authors would like to thank the astronaut Robert Louis Behnken from NASA, for the useful discussions. Authors are grateful to Professor Daniele Mortari, IEEE AESS distinguished lectures, Associate Professor of Aerospace Engineering at A&M Texas University, for the useful discussions and help during the seminar he animated in Sfax.

References

[1] Alex D., Bryan A., Sayed I., David I., Standard CMOS Active Pixel Image Sensors for Multimedia Applications, Sixteenth Conference 011 Advanced Research in VLSI, chapel heel north Carolina, 1995.

[2] Basak G., Micro-satellite camera design, master thesis, The Graduate School of Natural and Applied Sciences of the Middle East technical University, 2003.

[3] Canaan S H., On-Chip Spatial Image Processing with CMOS Active Pixel Sensors, Ph.d thesis, University of Waterloo, 2001.

[4] Gopalakrishnan V., Hridya V., Cypress S., «Integrate USB into image sensing applications», EE Times Design Articls, 2011.

[5] Jochua T., Implementation of a femto-satellite and a mini-launcher, Diploma thesis, polytechnic University of Cataluniya, 2010.

[6] Kashif G., Camera design for Pico and Nano satellite Applications, Master thesis, Lulea University of Technology, 2009.