NIOS II Processor Implementation In FPGA: An Application of Data Logging System

Ms. Sangita M. Pokale, Ms. K. A. Kulkarni, Prof. S. V. Rode

Abstract:- This paper present an application study in data logging device.The new kind of soft-core processor was designed based on NIOS II technology. The device make use of NIOS II processor provided by ALT ERA to be implemented in FPGA.NIOS II is a versatile embedded processor family that presents high performance and has been created for FPGA. Author targets implementation NIOS II soft core processor from Altera FPGA Platform. Also one of the FPGA vendor XILINX, are providing MicroBlaze & PicoBlaze RISC architecture. This is of 32 bit processing architecture. Author has implemented one simple digital circuit design on implementation of 8 bit asynchronous counter along with multiplexed seven segments LED Display Driver. Paper shows comparison on HDL based SOPC designing and usual discrete level hardware designing and testing. For HDL based circuit design Xilinx synthesis tool version 9.1 was used. Also after having success in this implementation author has implemented NIOSII soft core processor using QuartusII 10.1 & SOPC Builder Tool from Altera.

Index Terms:- FPGA CYCLONE III CPLD, NIOS II Soft Core Processor,Picoblaze,SOPC builder.

1 INTRODUCTION

A softcore processor is a microprocessor core that can be wholly implemented using logic synthesis.It can be implemented via different semiconductor devices containing programmable logic (e.g FPGA,CPLD). There are several soft cores available in the market, e.g. PicoBlaze, MicroBlaze, Openfire, Nios, Nios II, Cortex-M1, Mico8, Mico32. Out of all listed here PicoBlaze and mico8 are the 8-bit open source soft-cores available in the market. dozens of 8-bit microcontroller architectures and instruction sets. Modern FPGAs can efficiently implement practically any 8-bit microcontroller, and available FPGA soft cores support popular instruction sets such as the PIC, 8051, AVR, 6502, 8080, and Z80 microcontrollers. Authors have chosen CPLD because of availability of Xilinx tool chain. These design uses advance system on programmable chip(SOPC) technology with 32 bit NIOS II soft-core as the core to achieve well data login for time and temperature which has widely replaced the current structure of MCU or DSP the interface circuit is integrated in the field programmable gate array(FPG A)and the structure is simple.At the same time,because of the features which NIOS II can be configurated with FPGA.

- Ms. Sangita M. Pokale, P.G. Student (M.E. Digital Electronics), SIPNA's College of Engg. & Tech. Amravati (M.S.) India.
  Email – smpokle@rediffmail.com
- Ms. K.A.Kulkarni, P.G. Student (M.E. Digital Electronics), B.N. College of Engg., Pusad (M.S.) India,
  Email – kul_kashmira24@redliffmail.com
- Prof. S.V. Rode, Dept.of Electronics & Telecommunication, SIPNA's College of Engg. & Tech., Amravati(M.S.) India.
  Email – sandeeprode_30@yahoo.com

2 BACKGROUND

The PicoBlaze & NIOS II microcontroller is specifically designed and optimized for the Spartan-3, Virtex-II, Virtex-II Pro, Cyclon, Stratix FPGA architectures. Its compact yet capable architecture consumes considerably less FPGA resources than comparable 8-bit microcontroller architectures within an FPGA. Furthermore, the PicoBlaze & NIOS II microcontroller is provided as a free, source-level VHDL file with royalty-free re-use within Xilinx and Altera FPGAs. Even wide variety of Windows and Linux based assemblers and simulators are freely available for PicoBlaze and NIOS II. processing. The PicoBlaze microcontroller is optimized for efficiency and low deployment cost. It occupies just 96 FPGA slices, or only12.5% of an XC3S50 FPGA and a miniscule 0.3% of an XC3S5000 FPGA. In typical implementations, a single FPGA block RAM stores up to 1024 program instructions, which are automatically loaded during FPGA configuration. Even with such resource efficiency, the PicoBlaze microcontroller performs a respectable 44 to 100 million instructions per second (MIPS) depending on the target FPGA family and speed grade.

3 FPGA DEVELOPMENT TOOLS

In this project FPGA kit ALTERA DE2 has been employed .This board has an EP3C16F484C6 FPGA from cyclone III family.The main project software used is ALTERA QUARTUS II 10.1 WEB Edition.At this program all hardware description languages (HDL) like VHDL and VERILOG.The EP3C16F484C6 FPGA has some interesting hardware features that can be used in the design.

4 DESIGN OF HARDWARE SYSTEM

SOPC stands for System On Programmable Chip. Now a day's technology is growing faster and faster. Expectations of human from machine are increasing. This lead to increase in complications in hardware and more and more skills are required from hardware. In old days engineers were designing circuits and then they used to implement on the PCB's or bread boards. As those circuits were small so it was possible to implement practically. But think about the microprocessors used in our desktop computers which uses millions of transistors or millions of logic gates, is it possible to implement or test like with older methods? Answer is may be possible, but we cannot expect desired outputs or implementation and

production will be quick, as per the requirement of industries. Also many times integrated circuits which are made to for specific use. But we want some additional functionality in it. It is not possible to have custom designed integrated circuits ate low quantities as manufacturing cost is in millions of dollars. Often while using many microcontrollers we had seen that one particular vendor is providing some good feature but that is not available in the controller which I use. And for industries it is not possible to change the technologies they are using as designing new system takes too much time for research and it requires lot of funding. SOPC allows designer to have facility of making own design, required features within less interval of time. It is one time investment for companies. With the help of SOPC companies may upgrade their existing designs with change in hardware description language code. This saves lot of new hardware and money of the companies. With this technology functionality of complex systems can be made more complex very easily within small time span. In older systems as per the block diagram (Fig 1) shown we can see any general system, which is having so many things in the design. So the system is very bulky and costly. And the designed system may not be able to give proper performance.
But if we see the block diagram (Fig.2) how system gets reduced. Small system will give optimized performance.
While designing small system errors can be minimized or debugged very easily.

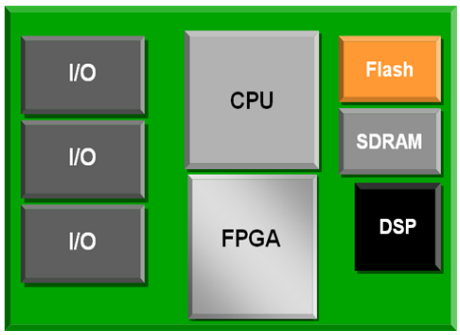

Fig.1

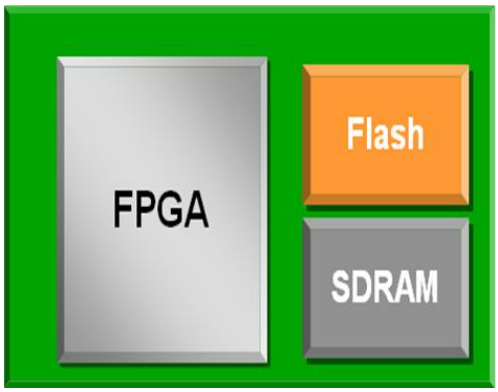

Fig.2

5 IMPLEMENTATION

We are doing research on SOPC designing and we have implemented one such design by hardware and SOPC based approach. We designed simple counter and driver circuit for handling multiplexed seven segments display. Block diagram shown in Fig 3. Block diagram shown Fig. 4 shows with the help of SOPC how complications of the circuit can be reduced.

Furthermore having on chip Soft-core NIOSII processor to improve efficiency, reduce the design time & complexity implemented on Altera's CycloneIII series FPGA. For this implementation DE0 Board was used. Typical application of high speed data logger was implemented using NIOSII soft-core processor. In this demonstration job of NIOSII processor is to read data from ADC0804 and logs to the Pen Drive. To interface Pen Drive to FPGA (NIOSII) VNC1L USB Host Controller was used. VNC1L was interfaced by UART interface.

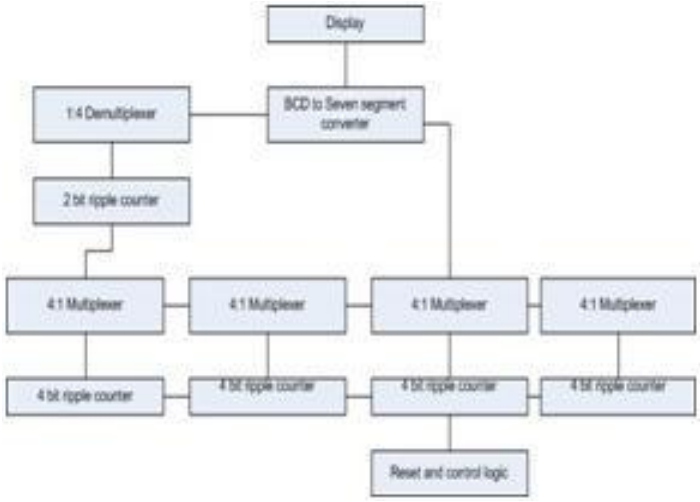

Fig. 3

Fig. 3 shows the block level design of the counter. Number of block represent number of disctere devices.

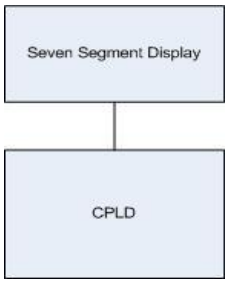

Fig.4

The SOPC builder provide as a system platform for setting two level modules .
1. Top level design &
2. Low level design.
Top level design:

Fig.5 :Block diagram high level

The major hardware circuit is designed based on the hardware resources of DE 2 development board.It regards the EP 2c35 f672c6 FPGA as the main chip .It achieves connections of the various IP core through the SOPC builder in QUARTUS II, completes the work of NIOS II SOFT-CORE and associated peripherals.The embedded processor attached to NIOS II family is a kind of general CPU of RISC structure which can be configured by the user. The NIOS II structure among the design includes NIOS II ,UART,LCD etc,peripherals can be added by SOPC builder development tool according to actually need, and the number is not limit.Component editor is an important part of SOPC builder .It allows us to create and edit their own components.

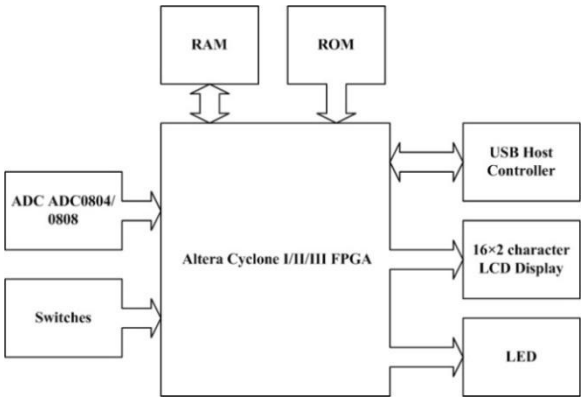

Fig.6

Fig. 6 shows block diagram of desired NIOSII based data logging application. Using NIOSII soft-core processor, standalone data logging system is implemented. Job of NIOSII processor is to read data samples from ADC periodically and to store the data on the pen drive or USB mass storage device with time stamp. To achieve real time requirements and data processing, uC OSII Real Time Operating System (RTOS) is implemented. With the help of operating system, multiple tasks can be performed.

The tasks can be:

- Handle real time clock
- Display current time
- Get settings from user through switches
- Display settings and information on LCD.
- Read data from ADC
- Handle USB host controller

6 DESIGN FLOW

Development of this project is in two phases.

Phase 1: Hardware design flow

Implementation & Simulation in Quartus II:

The Altera Quartus II design software provides a complete, multiplatform design environment that easily adapts to your specific design needs. It is a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes solutions for all phases of FPGA and CPLD design. In addition, the Quartus II software allows you to use the Quartus II Graphical user interface and command-line interface for each phase of the design flow.

The Quartus II software includes a modular Compiler. The Compiler includes the following modules (modules marked with an asterisk are optional during a compilation, depending on your settings):

- Analysis & Synthesis
- Partition Merge
- Fitter
- Assembler
- Time Quest Timing Analyzer
- Design Assistant
- EDA Netlist Writer
- HardCopy Netlist Writer

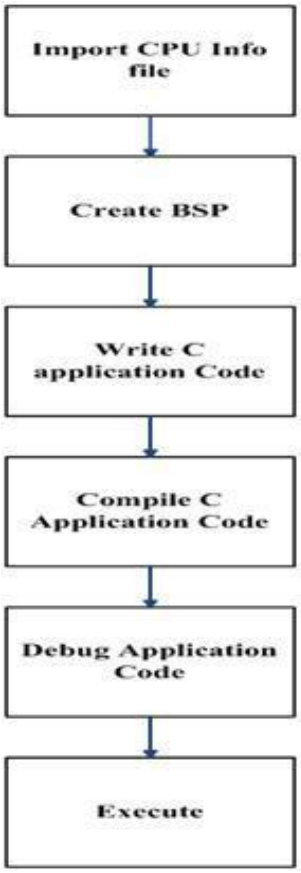

Fig.7: ***Software design flow***

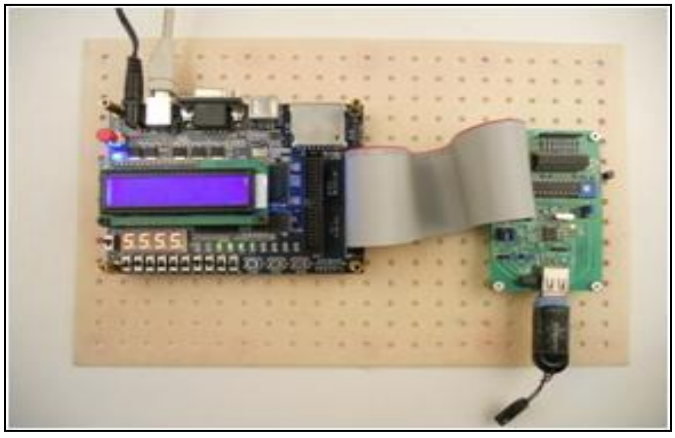

Fig.8

Fig. 8 shows final implementation of the data logger system

using SOPC concept.Figure shows the result of our research and experiment.The softcare processor using FPGA is designed and implemention of data logger system using SOPC concept is shown.

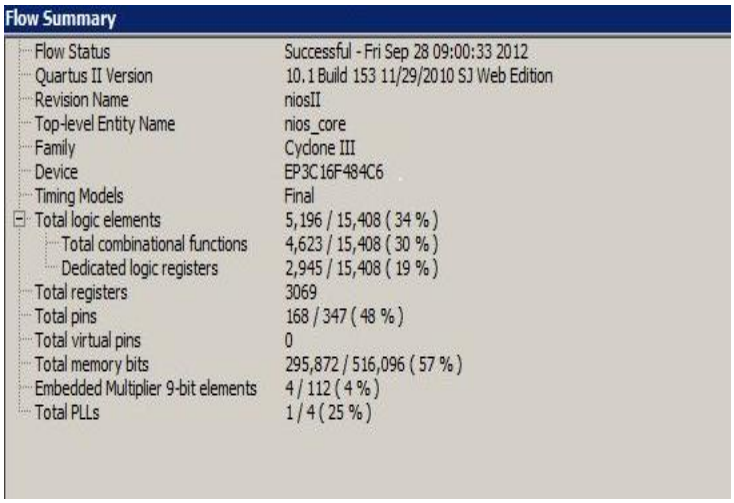

Fig.9

Fig. 9 shows the design analysis report in terms of resources used.We have used Easy Start CPLD board from UC Micro Systems India for XC95108 and Xilinx ISE 9.1 tool for synthesis and implementation and QuartusII 10.1 edition was used to implement NIOSII soft-core .

7 CONCLUSION

The Embedded System can be implemented on FPGA directly with the help of HDL. System optimization can also be done with the same. As design utilized only34% resources so we can add multi core and DSP co processor to enhance the system without extra efforts.

REFERENCES:

1) NIOSIIDocumentation: www.altera.com/products/ip/processors/nios2.

2) Quartus II Software information and download. http://www.altera.com/products/software/quartus-ii

3) WikiReference: http://en.wikipedia.org/wiki/Soft_microprocessor.

4) Altera DE0 Board vendor: http://www.terasic.com.tw

5) Tutorials for NIOSII implementation: http://www.doulos.com/content/training/altera_niosII_training.php

6) Application Research of Nios II Technology on Logging Device of Ground: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5661289

7) Hardware-AcceleratedNIOS-II Implementation of a Turbo Decoder: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5380477