

# Analysis And Characterization of Different Comparator Topologies

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**Abstract:-** Comparator is one of the most important analog circuits required in many analog integrated circuits. It is used for the comparison between two different or same electrical signals. The design of Comparator becomes an important issue when technology is scaled down. Due to the non-linear behavior of threshold voltage ( $V_T$ ) when technology is scaled down, performance of Comparator is affected. Many versions of comparator are proposed to achieve desirable output in sub-micron and deep sub-micron technologies. The selection of particular topology is dependent upon the requirements and application. In this paper, we have shown the implementation of different topologies in  $0.5 \mu\text{m}$  technology using the Mentor Graphics Tool. We have done the pre-layout simulation of two different topologies. We have performed DC, AC and transient analysis. We have also calculated output impedance. We have prepared a comparative analysis about them.

**Keywords:-** Voltage Gain, Output Impedance, Output Voltage Swing, Power Dissipation.

## I INTRODUCTION

The schematic symbol and basic operation of a voltage comparator are shown in Fig. The comparator can be thought of as a decision-making circuit. If the +,  $v_+$  input of the comparator is at a greater potential than the -,  $v_-$ , input, the output of the comparator is a logic 1, whereas if the + input is at a potential less than the - input, the output of the comparator is at a logic 0. Although the basic op-amp of the last chapter can be used as a voltage comparator, in some less demanding low-frequency or speed applications, we will not consider the op-amp as a comparator. Instead, we will discuss practical comparator design and analysis where propagation delay and sensitivity are important.

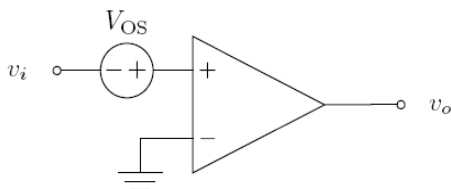
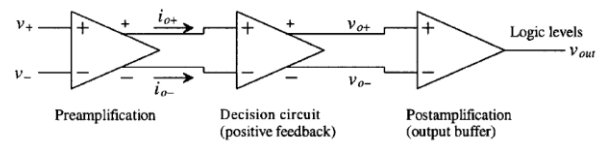


Fig 1. Basic Comparator Symbol

A block diagram of a high-performance comparator is shown in Fig.2. The comparator consists of three stages; the input preamplifier, a positive feedback or decision stage, and an output buffer. The preamp stage (or stages) amplifies the input signal to improve the comparator sensitivity (i.e., increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise coming from the positive feedback stage (*this is important*).

The positive feedback stage is used to determine which of the input signals is larger. The output buffer amplifies this information and outputs a digital signal. Designing a comparator can begin with considering input common-mode range, power dissipation, propagation delay, and comparator gain.



## II Basic Comparator

The most basic version of the Comparator is the source follower. It is a common drain amplifier circuit with unity voltage gain. The output at the source terminal follows the input applied at the gate. The schematic of the circuit is shown in fig.1. It is designed with the NMOS, PMOS and ideal current source. We can use current mirror also in place of current source. Comparator can also be designed with the resistor connected between source and supply. But it does not allow a constant current flowing through the source terminal. It results into non-linearity in the output and we can't achieve unity voltage gain always. It also has high output impedance. So, resistive configuration is not used. We can use PMOS or NMOS as a load. But, the implementation with current mirror provides good results.

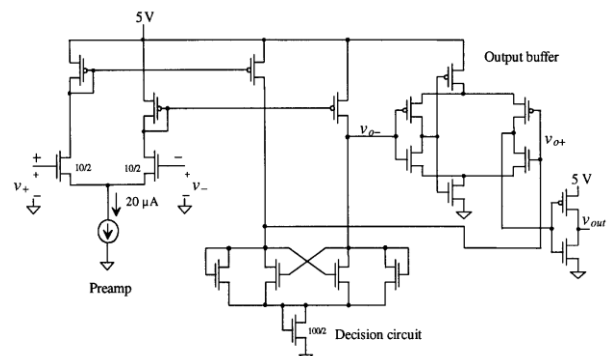


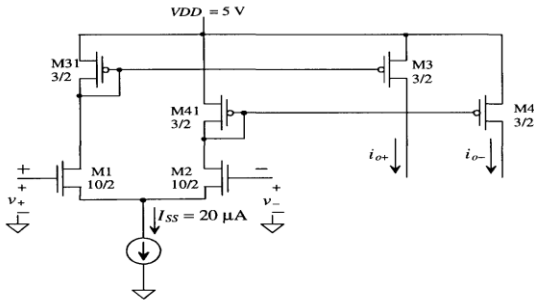
Fig 2.1. Basic comparator

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The supply voltage requirement with is either 3.3V or 5V. In the basic source follower, the PMOSFET works in the saturation region since  $V_{DS} \leq V_{GS} - V_{TH}$ .

The most important parameter of Comparator is its output impedance. We can derive it from the small signal model shown in the fig.2.2 [6][9][10][18].

**2.1 Pre-amplification Stage:**



**Fig 2.2. Pre-amplification circuit**

For Pre-amplification stage, it is important to concentrate on speed only so we are keeping length of channel to 2um for M1 and M2. Using size shown in schematic we can relate input voltage to output current, Here (W/L) of M1 and M2 is (10/2).

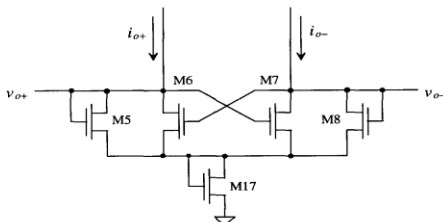
$$i_{o+} = g_m/2 (V_+ - V_-) + I_{ss}/2 = I_{ss} - i_{o-} = 20\mu A - i_{o-}.$$

In this design case,

$$g_m = g_{m1} = g_{m2} = \sqrt{2 \left(\frac{10}{2}\right) 50 \frac{\mu A}{V^2} 10 \mu A} = 71 \mu A/V.$$

In other words, if  $V_+$  is greater than  $V_-$  by 10mV then,  $i_{o+}$  And  $i_{o-}$  will be 10.35 and 9.65 mA respectively. The desired output gain can be obtained by adjusting W/L ratios of two transistors M3 and M4.

**2.2 Decision Making stage:**



**Fig 2.3. Decision Making Circuit**

The decision-making-circuit is the heart of the comparator and should be capable of differentiating between [3]mV level signals. We should be able to create a design of the circuit with some hysteresis for use in rejecting noise on a signal. The circuit used in the present comparator is shown in Fig 2.3[3]. The circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element[3]. Let's begin by assuming that  $i_{o+}$  is much larger than  $i_{o-}$  so that M5 and M7 are on and M6 and M8 are off. We will also assume that  $\beta_5 = \beta_8 = \beta_A$  and  $\beta_6 = \beta_7 = \beta_B$ . Under these circumstances,  $v_{o-}$  is approximately 0 V and  $v_{o+}$  is

$$v_{o+} = \sqrt{\frac{2i_{o+}}{\beta_A}} + V_{THN}$$

If we start to increase  $i_{o-}$  and decrease  $i_{o+}$  switching takes place when the drain-source voltage of M7 is equal to  $V_{THN}$  of M6. At this point, M6 starts to take current away from M5. This decreases the drain-source voltage of M5 and thus starts to turn M7 off. If we assume that the maximum value of  $v_{o+}$  or  $v_{o-}$  is equal to  $2V_{THN}$ , then M6 and M7 operate, under steady-state conditions, in either cutoff or the triode regions. Under these circumstances, the voltage across M7 reaches  $V_{THN}$ , and thus M7 enters the saturation region, when the current through M7 is

$$i_{o-} = \frac{\beta_B}{2} (V_{o+} - V_{thn})^2 = \frac{\beta_B}{\beta_A} i_{o+}$$

This is the point at which switching takes place; that is, M7 shuts off and M6 turns on. If then switching takes place when the currents,  $i_{o-}$  and  $i_{o+}$  are equal. Unequal ps cause the comparator to exhibit hysteresis. A similar analysis for increasing  $i_{o+}$  and decreasing  $i_{o-}$ ; yields a switching point of Relating these equations to Eq. yields the switching point voltages

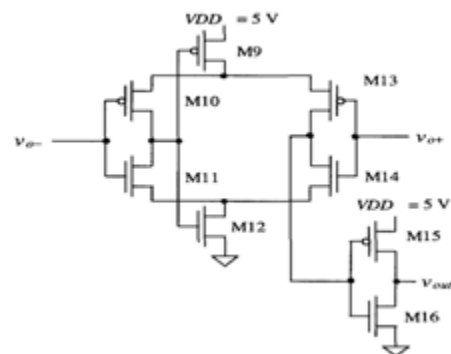
$$V_{SPH} = v_+ - v_- = \frac{I_{ss} (\beta_B - \beta_A)}{g_m (\beta_B + \beta_A)}; (\beta_B \neq \beta_A)$$

and

$$V_{SPL} = -V_{SPH}$$

**2.3 Output Buffer:**

The final component in our comparator design is the output buffer or post-amplifier. The only purpose of the output buffer is to convert the output of the decision circuit into a logic signal[3](i.e., 0 or 5 V). The output buffer should accept a differential input signal and not have slew-rate limitations.



**Fig 2.4. Output Buffer Circuit**

The circuit used as an output buffer in our basic comparator design is shown in Fig. 2.4. This circuit is a self-biasing differential amplifier. An inverter is added in the output of the amplifier stage as an additional gain stage and to isolate load capacitance from the self-biased differential amplifier. The input  $v_{o+}$  is swept from 1 to 4 V, while  $v_{o-}$  is held at 1 to 3.5 V in 0.5 V increments. It is apparent that the

inputs,  $v_{o+}$  and  $v_{o-}$  should lie within 1.5 and 3 V for linear operation of the output buffer. Comparing this result with the output of the positive feedback circuit, which varies from 0 to 1.5 V, we see a problem in connecting the decision circuit directly to the output buffer. For shifting the output of the decision circuit up approximately 1V, the circuit shown in Fig. 2.3 is used. The MOSFET M17 is added in series with the decision circuit to increase the average voltage out of the decision circuit. The size of the MOSFET is somewhat arbitrary. We will set  $W_{17}/L_{17} = 100\mu\text{m}/2\mu\text{m}$ . so that the output of the decision circuit is increased by approximately  $V_{THN}$ . The complete schematic of the comparator is shown in Fig.2.1. Unlabeled MOSFETs are 3  $\mu\text{m}/2\text{ urn}$ .

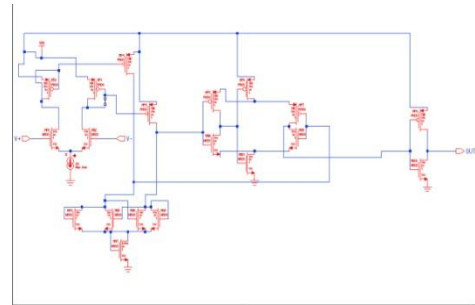


Fig 2.7. Basic Comparator

**III SELF BIASED COMPARATOR**

For the final example of a comparator, consider the self-biased comparator shown in Fig.3.1 [1]. This circuit operates similar to the self-biased differential amplifier but with a larger gain and wider input common-mode range. Note that because of the high gain of this comparator configuration, the delay tends to be longer (hundreds of ns) than the other configurations we discussed. The delay can be reduced, at the price of gain and more power dissipation, by decreasing the widths of M1 through M4 (operating M1 through M4 in the triode region) and by using minimum channel lengths.

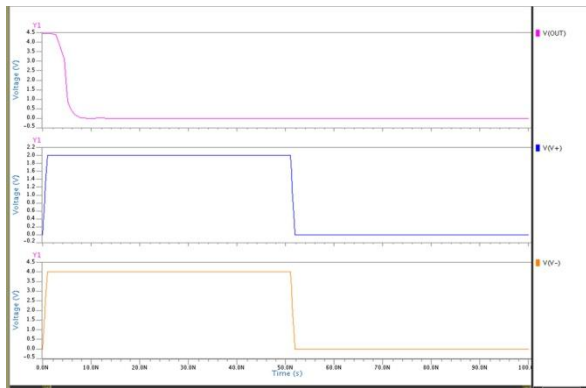


Fig 2.5. Transient Analysis of Comparator

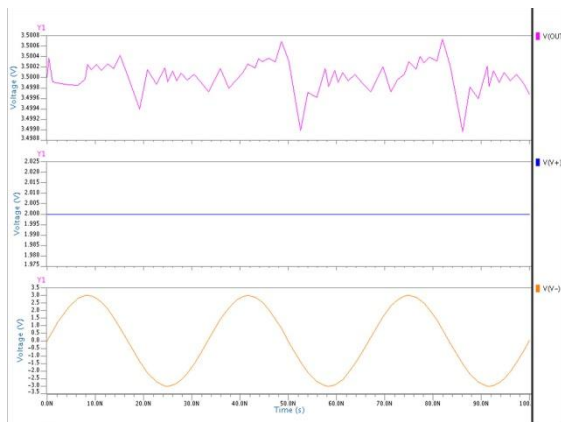


Fig 2.6. Transient Analysis of Comparator

The table based on simulation results of Comparator is shown in table-1.

**Table I.**  
**Simulation Results of Comparator**

Parameter	Value
Voltage Gain	2000
Offset Voltage	2.2022 mV
Operating Voltage Range	3.5 to 5 V
Bandwidth	30 MHz
Number of Transistors	17

The implementation of Basic Comparator is shown in fig2.7 [1].

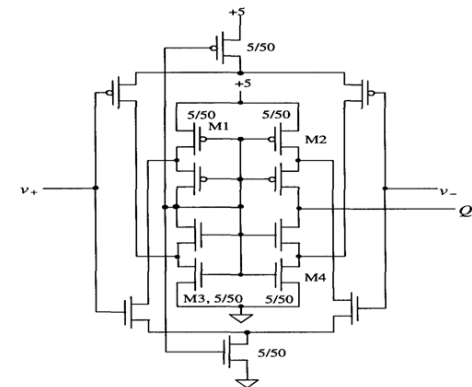


Fig 3.1. Self Biased Comparator

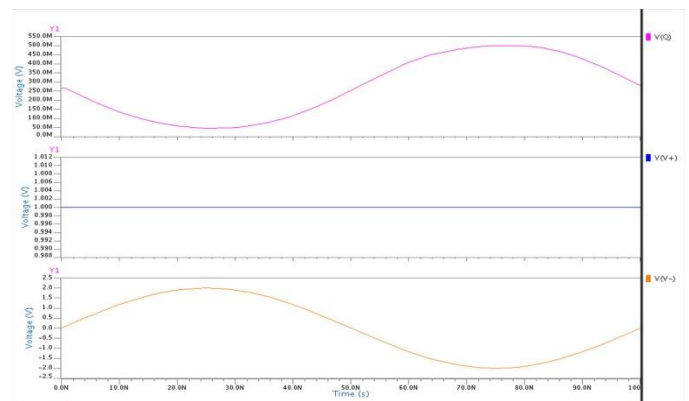


Fig 3.2 Transient analysis of Self Biased Comparator

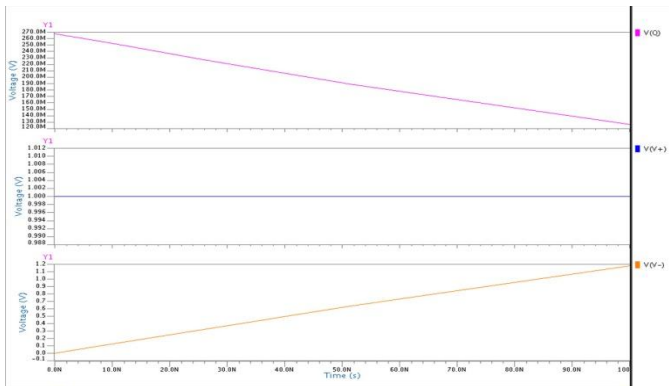


Fig 3.3 Transient analysis of Self Biased Comparator

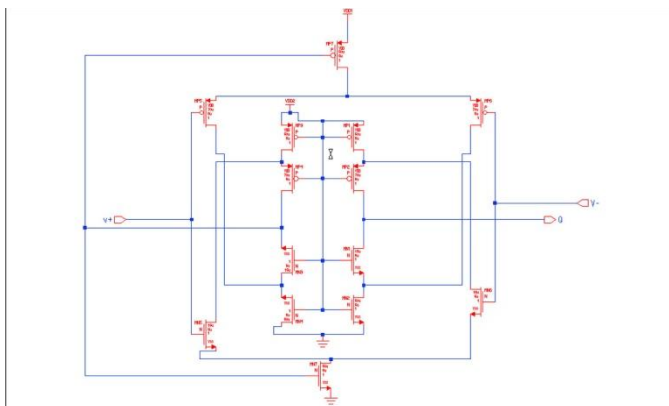


Fig 3.4 Self Biased Comparator

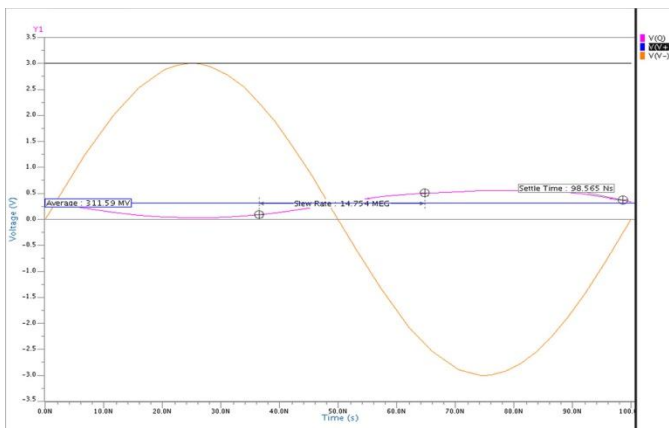


Fig3.5 A.C. Analysis of Self Biased Comparator

Table-2 shows the simulation results of Self-Biased Comparator.

Parameter	Value
Voltage Gain	3000
Propagation Delay	0.324us
Gain Margin	10.172Db
Bandwidth	23.0880 MHz
Number of Transistors	14

The number of transistor of Self Biased Comparator is decreased to 14, it decreases the size. So it limits the output swing in deep sub micron technology. This is the major disadvantage of Self Biased comparator topology.

### IV COMPARATIVE ANALYSIS

Table 3  
Comparative Analysis

Topology	Voltage Gain	Bandwidth	No. Of Transistors
Basic Comparator	2000	30MHz	17
Self Biased Comparator	3000	23.0880 MHz	14

The comparative analysis of all two topologies is shown in table-3. It explains the advantages and disadvantages of all three circuits. Output impedance is low and better in case of threshold independent Comparator and Self Biased Comparator. Bandwidth is higher in case of Basic Comparator has high power dissipation because of requirement of large biasing current. Both topologies provide approximately high voltage gain.

### V CONCLUSION

This paper explains about the Comparator and its design in sub-micron and deep sub-micron technologies. The three topologies of voltage followers have been implemented in 0.5 μm technology and brief comparison between them is made by analyzing pre-layout simulation results. The basic parameters need to be considered in any design is output impedance and voltage gain. Comparison table shows that different circuits have different advantages and disadvantages. Threshold independent Comparator provides zero offset voltage. It is having many advantages compared to the other versions. Still, But, the selection of any topology is based on the application and the requirements.

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