A Low-Cost Very Large Scale Integration Architecture For Idct With Sharing Techniques

S. Shunmugapriya, M. Saravanan

Abstract:- The intercommunications between the video devices using different standards are so much inconvenient, thus video codec supporting multiple standards are more useful and more attractive. In this brief, a low cost very large scale integration (VLSI) architecture is designed for multistandard inverse Discrete Cosine transform. It is used in multistandard decoder of MPEG-2, MPEG-4 ASP, and VC-1 .Two circuit share strategies, factor share (FS) an adder share (AS) are applied to the inverse transform architecture for saving its circuit resource. Pipelined stages are used in this Multistandard inverse transform to increase the operational speed.

Keywords:- *Hardware Share, multiple inverse transform, Video decoding,factor share,adder share.*

1. INTRODUCTION

Currently, several video compression standards, e.g.MPEG-2, MPEG-4ASP, H.264/AVC and VC-1(Windows Media Video 9), are widely applied in video codec products, such as digital TV, mobile video, video conference, and so on. Integrating multistandard encoding or decoding circuits into a single chip will increase the area and power consumed, which has a negative impact on the cost of the chip products. Thus, a critical problem that is needed to be solved in multistandard codecs is the increasing cost. It will be competitive that multistandard codecs achieve both high performance and low cost. The circuit share is an efficient method for the circuit resource reduction. The integration of multistandard codec does not mean that several standard codecs are simply gathered together. It is expected to have a higher density of integration by circuit share. Many coding tools from different compression standards are similar, even though their detail algorithms are different, such as motion estimation, inverse transform and inverse quantization, and variable length decoding. Similar coding tools from different standards may be efficiently integrated in a single chip through elaborating circuit share, so that the area of the integrated multistandard chip is much smaller than the total areas of these single standard chips. Discrete cosine transform (DCT) is a key coding tool for video compression. It achieves data compression by converting the high relative spatial domain data into low relative frequent domain data. In this project, a low cost very large scale integration (VLSI) architecture is designed for multistandard inverse transform. It is used in multistandard decoder of MPEG-2, MPEG-4 ASP, and VC-1 .Two circuit share strategies, factor share (FS) an adder share (AS), are applied to the inverse transform architecture for saving its circuit resource.

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2. CIRCUIT SHARE STRATEGIES

2.1 FACTOR SHARING

The circuit area can be efficiently reduced by adopting appropriate circuit share strategies. Multiplication operations are needed in traditional IDCT processing. However, the circuit of multiplier is relatively complicated for VLSI implementation. Thus, the multiplier-less transform is preferred. In the multiplier-less transform, each element of the IDCT matrix is equally expressed as the sum of several binary factors. The expression can be friendly implemented with additions and shifts in the digital system. Although some elements in the integer IDCT matrix are different, some sums of their binary factors (SBFs) are possibly the same. The same SBFs can be shared in the multiplier-less implementation of the integer IDCT. This circuit optimization strategy is called as FS. FS helps to avoid the repeating circuit implementations of these same SBFs.

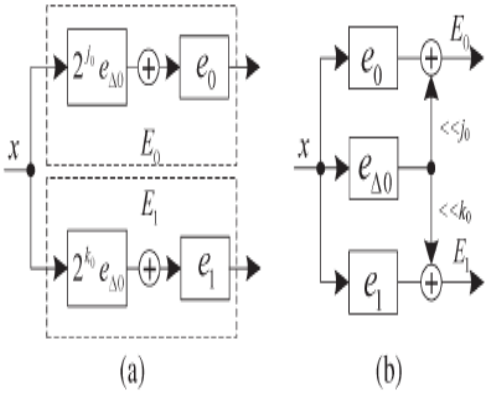

Figure1. Circuit of element factorization (a) without FS (b) with FS

Figure 1 shows the circuit element factorization without Factor Sharing and with Factor Sharing. Different binary factorization forms have different share factors eΔ. However, it is fortunate that the elements of the IDCT are usually not complicated. It is possible to obtain an optimal or near-optimal eΔ reducing the circuits as possible. Figure 2. shows the Circuit architecture of bcde(x) of MPEG-2/4 8-point IDCT based on Factor Sharing.

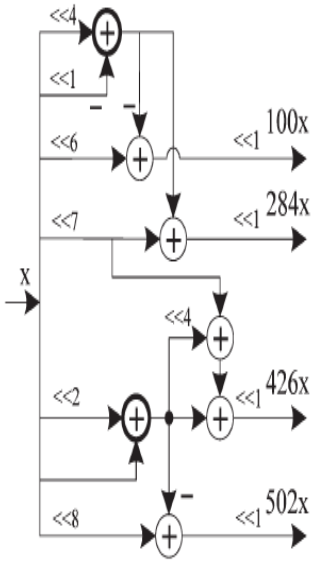

Figure 2 Circuit architecture of bcde(x) of MPEG-2/4 8-point IDCT based on FS

2.2 ADDER SHARING

In the multiplier-less implementation of IDCT, the adder consumes more circuit resources than other operators; thus, AS is employed to share the adders among different IDCTs.Figure3shows the Circuit of element factorization without Adder Sharing, and with Adder Sharing.

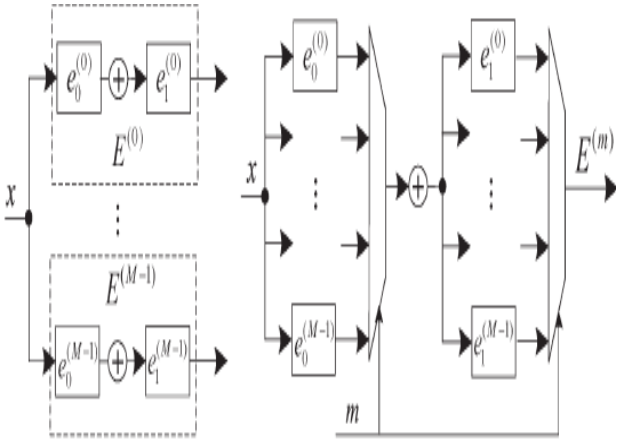

Figure 3. (a) Circuit of element factorization without AS, (b) with AS.

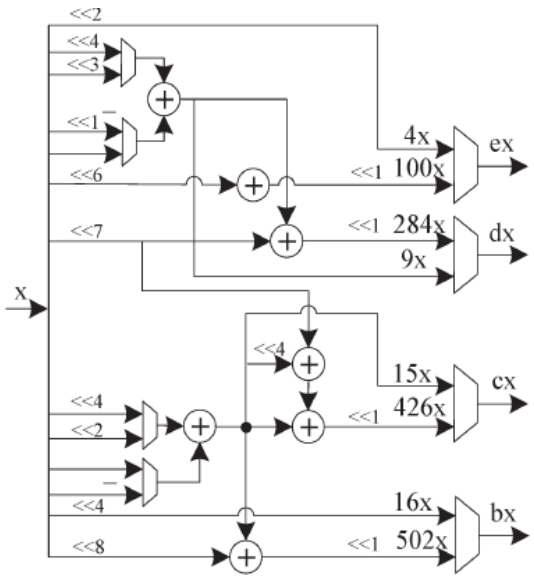

Figure 4. architecture of the bcde(x) of integrating MPEG-2/4and VC -1 IDCTs based on AS

Figure 4 shows the Circuit architecture of the bcde(x) of integrating MPEG-2/4and VC -1 8point IDCTs based on AS and Figure 5 shows the VLSI architecture of 1-D multistandard IDCT

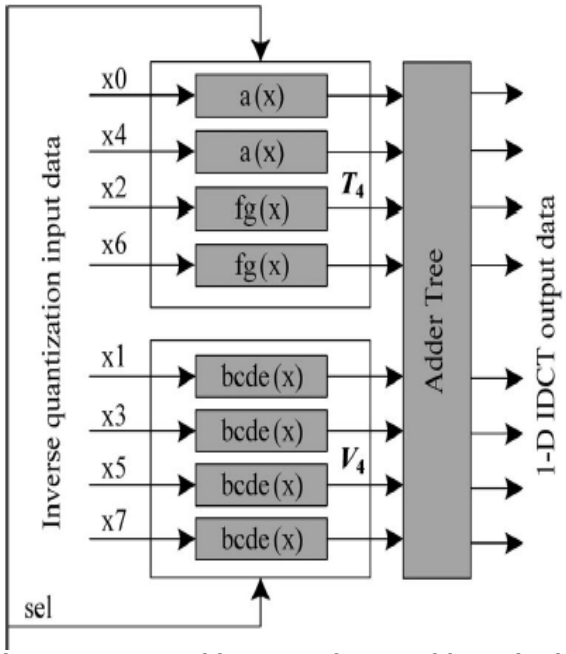

Figure 5. VLSI architecture of 1-D multistandard IDCT

3. SIMULATION RESULTS

3.1WAVE FORM FOR BCDE

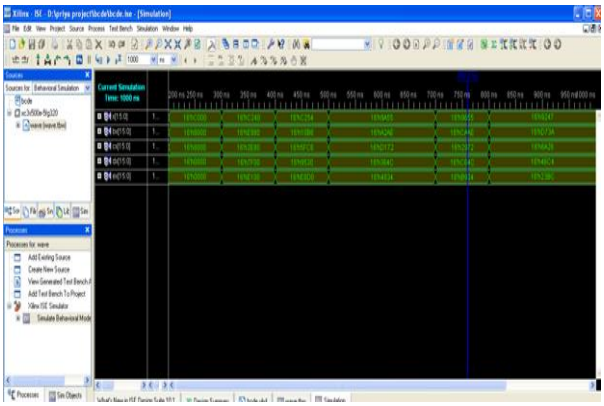

Figure 6. Output waveform for subunit bcde

Figure 6 shows the output waveform of subunit bcde .In this x1,x3,x5,x7 are the input of bcde and outputs are bx,cx,dx,ex then seven adders are used in this bcde unit This bcde unit is used to design the 1-D multistandard IDCT.

3.2 WAVE FORM FOR AFG

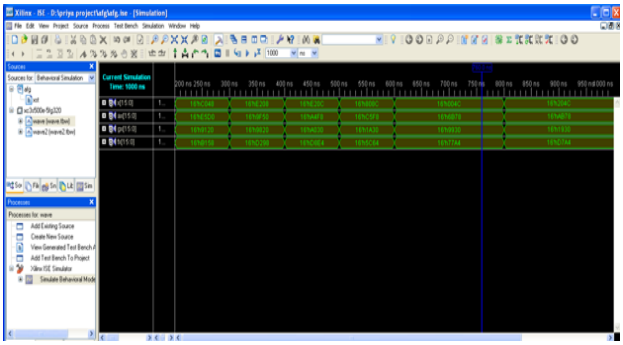

Figure 7 Output waveform for subunit afg

Figure 7 shows the output waveform of subunit afg.In this x0,x2,x4,x8 are the input of subunit afg and outputs are ax,fx,gx. Three adders are used in ax and Five adders are used in fgx

3.3 WAVE FORM FOR IDCT

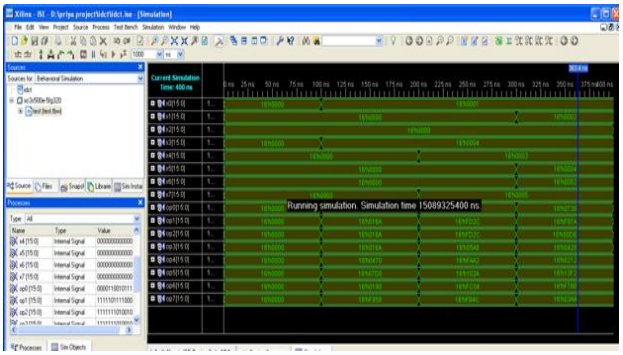

Figure 8. Output waveform for IDCT

Figure 8 shows the output waveform of the 1-D multistandard IDCT.It consist of bcde and afg sub units. x0,x2,x4,x6 are the inputs of afg and x1,x3,x7,x5 are the inputs of bcde.T4 andV4 are the output of afg and bcde.t4,v4 are given to the adder tree then it produce IDCT output.

3.4 PIPELINED IDCT

To achieve efficient hardware shares with IDCT, we use the inverse transform matrix in AVS to reduce the hardware cost and computational complexity for the IDCT design.The purpose of the hardware sharing design is to reduce the hardware cost when the multiple inverse transforms are used for the multiple-standard video decoder. Pipelined stages are used to increase the operational speed .

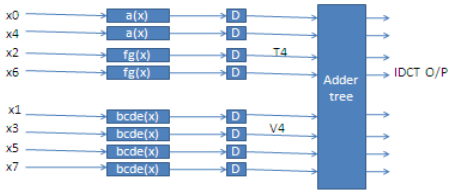

Figure 9. VLSI Architecture of Pipelined IDCT

3.4.1 COMPARISON TABLE

PARAMETER	NORMAL V4	PIPELINED V4
DELAY	20.50	16.82

Figure 10.Delay Comparison Table

3.4.2 COMPARISON GRAPH

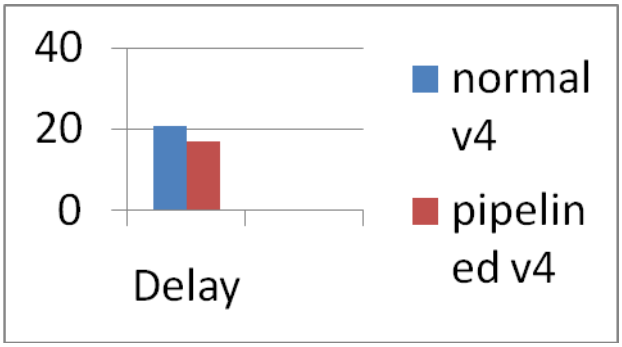

Figure 10.Delay comparison graph

3.5 WAVE FORM FOR PIPELINED IDCT

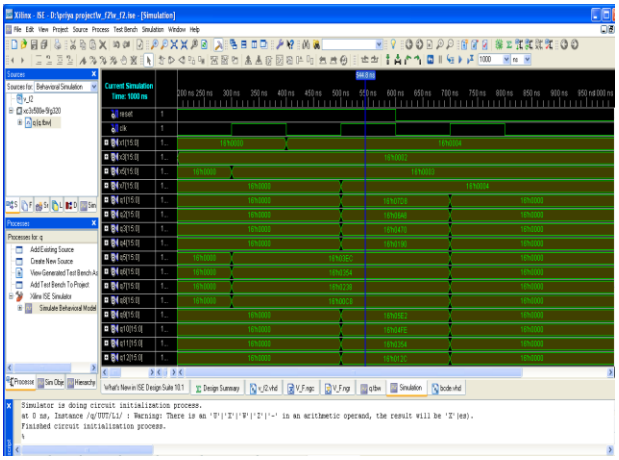

Figure11.Output waveform for pipelined IDCT

4. CONCLUSION

IDCTs of several standards are integrated in the proposed architecture. The circuits are efficiently shared and saved based on the FS and AS strategies. For the hardware sharing design of the fast 1-D 4 × 4 and 8 × 8 integer transforms, the common hardware modules are shared to reduce the total hardware costs. Thus, the hardware costs of the proposed 1-Dand 2-D hardware-sharing designs are smaller than those of the individual and separate designs without shares. It can be concluded that a high decoding capability is achieved in small IDCT architecture area. With the hardware share, the proposed architecture is suitable for the low-cost implementation of the VC-1,MPEG-2,MPEG-4 ASP,H.264/AVC codec.

5. AKNOWLEDGEMENT

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