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Analysis Report of Gate Driver Circuit for TFT-LCD

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Abstract

Gate driver circuit for TFT LCD can be designed by different technique such as standard five mask process designed on glass substrate using coupled clock logic, center offset technique, integrated five transistor & one capacitor approach with a silicon hydrogenated in multi phase clock mode, combination of a-Si:H process. This paper presents brief analysis of this application on the basis of following parameter by such as capacitor coupling effect, threshold voltage shift, and power consumption, life time of gate driver, floating row lines, driving speed & output stability.

Keywords: Threshold voltage shift, Power consumption, Stress effect, Fluctuation noise.

I. Introduction

This paper defines the fundamentals of a gate driver circuit & also helps to estimate best technique for gate driver circuit for TFT-LCD. At the beginning of display technology for more than four decades CRT display has been used, the last two decades flat panel display (FPD) technologies could replace CRT display.

In late 1990 was a milestone year of display technology where TFT-LCD being popular. In the starting when LCDs were used in small sized display direct or passive matrix addressing method were using, as the size & resolution were increased the number of pixel also increased, due to this requirement new addressing technique were required. This requirement fulfill by adding a switch TFT at each pixel of the display matrix. In this technique first external voltage controls whether the switch is ON or OFF, the second voltage is used as a bias voltage which is store in capacitor. The storage capacitor provides voltage to the liquid crystal if it's parallel connected, this capacitor maintains required voltage across liquid crystal constantly during frame time. This type of addressing is called AMLCD. For manufacturing AMLCD gate driver different techniques are used such as

1. Glass substrate technique was used for design integrated TFT Gate driver with coupled clock logic which helps reduce the stress effect in to the pull down branches & fluctuation in output voltage also decreases.
2. Two major problem may affect the performance of conventional gate driver circuit one is output fluctuations (due to floating) by which row lines are float & second is capacitor coupling effect at pull up circuit. For solving these problems AC or DC biasing technique were used.
3. Stability of gate driver circuit & the threshold voltage shift Vth is another major issue during circuit operation. To overcome these problems center offset technique were used as a switching device in AMLCD.
4. The concept of SR latch gate driver circuit is used in AMLCD. This technique is based on a standard five mask process in this technique ten TFT's & two capacitor are used for composing pull up network by reducing the Vgs voltage of a pull down TFT, the proposed SR latch gate driver can prevent Vth shift.
5. Full scale pre-charge voltage is a new scheme which is used as an input; it shows the improvement in driving speed of the gate driver circuit.
6. For getting better performance novel low power gate driver circuit has been designed. In this gate driver circuit integrated approach of five mask process & a-Si:H with an Ac driving method being used. In this technology clock modification also applied which gives better result in comparison to all above mention technologies in the form of low temperature processing, low cost, better coverage across large substrate area. The vth shift decreases by using an ac driving method it gives benefit in the form of stabilize output waveform and prevents the row line from floating. It also reduces the power consumption by decreasing the switching time of clock signal.

II. Technical summary

1) The conventional gate driver circuit suffers stress effect. To overcome this problem doubling the pull down branches in place of single pull down branch but it can't provide satisfactory improvement. Glass substrate technique has tried to suppress this problem by the anti fluctuating structure [8]. It helps to control the dual pull down structure with a reduced gate voltage on the pull down transistor & for controlling gate driver two phase clocks (coupled clock) is used.

In above scheme one of two pull down transistor is turned on alternatively after half time of clock signal for full fill the low output voltage of gate driver. Further improving the stress effect of transistor two another technique being adopted one is reducing turn on time & second is decreasing the control voltage but the area of circuit is increased and circuit becomes complex.

According to the result by using additional pull down transistor is helpful for low stress effect due to turn on time is reduced also suppress fluctuation noise at output node & output voltage reaches up to 15v but the life time of gate driver is less in comparison to previous work .

2) Capacitor coupling and defect creation may affect the performance of gate driver circuit in form of output fluctuation, which directly affect image quality. To overcome this problem DC biasing applies on pull down TFT. It eliminates floating row lines but introduces noise. Life time of gate driver is also reduced. To improving this problem AC driving method is used. In this method V_{th} shift can be minimized by controlling duty ratio (33.3% approximately) of gate bias stress [1], High voltage swing (V_{sw}) of clock signals is a major factor which will reduce lifetime of a-Si:H TFTs. so using Ac driving method output is stabilized against noise by modulating bias stress on pull down TFTs and give moderate V_{th} shift after long operating time at 100^0c.

3) Center offset technique focused on life time of a gate driver which depends on threshold voltage shift [1]. To improve stability of gate driver pull down TFTs should be stable because they protect floating row lines and bootstrapping node when output is in off state. In this technique pull down transistor operates alternately with 50% duty cycle i.e. when clock 1 goes high, output node charge through high input signal. During clock 2 voltage of output node boosted up due to capacitive coupling [10]. Therefore output signal is generated without change in V_{th} of pull up transistor after generating output voltage and output node is discharge through simultaneous pull down network when reset signal is applied, Due to above phenomenon center offset TFTs are used only in pull down network as a shift register to improve life time of driver circuit. Measurement result shows that output of pull-down transistor remain stable for $3x10^8$s & V_{th} shift of center offset TFTs is 35% smaller than that previous one.

4) Speed of gate driver circuit is one of the challenging task to overcome this problem bootstrapping method is proposed in which high gate to source voltage applied during pull up period due to this gate pulse time is much reduce so that conventional gate driver circuit does not achieve high speed requirement, for achieving high speed full scale pre charge voltage is better technique for gate driver circuit [8]. In this technique a diode is connected with conventional circuit. Proposed gate driver circuit consists of pull up network, pull down network and low level holding network. Those network made by 7 TFTs and two capacitors with two clock signals. Results verify improvement in driving speed of proposed circuit in comparison to conventional circuit.

5) Shift register is a basic building block of gate driver circuit. It is designed by SR latch by using standard five mask process [9]. In this approach two capacitor and ten transistors are used. Here the important issues are reduction in V_{th} shift [1], improvement in circuit operating stability. Those improvements are possible by adopting some major key points given below:

i. By applying reduced duty ratio of clock signal [9].
ii. By accelerating output node voltage at operating stage and it is being stabilized through V_{ss} at the end operation.
iii. Layout dimensions are reduced by minimizing the size of pull down TFTs subsequently.

If the proposed circuit uses ac driving structure which help to increase lifetime and prevents floating of row line. For achieving above described feature, clock signals are used and resultantly the pull down TFTs gets turn on. These TFTs discharge row lines. As far as above technique is concern circuit remains stable for more than 240 hours at high temperature (100^0C).

6) A novel low power gate driver circuit is used integration of above techniques and fabricated on glass by using a-Si:H with standard five mask process. The proposed gate driver circuit shows remarkable performance improvement in comparison to all above mentioned gate driver circuit in terms of output stability, uniform coverage area along large substrate, low V_{th} shift, low power consumption, high temperature performance during long operating time, and low fabrication cost.

Proposed gate driver circuit used an Ac driving method with 25% duty ratio which controls threshold voltage & also prevents row line from floating. Driving clock signal keeps pull down TFT's separately & continuously turn on which provide stabilize output for gate driver circuit. Proposed gate driver circuit use low frequency (~0.25) i.e. switching time of clock signal is less in comparison to previous work by which power consumption of proposed gate driver circuit is reduced.

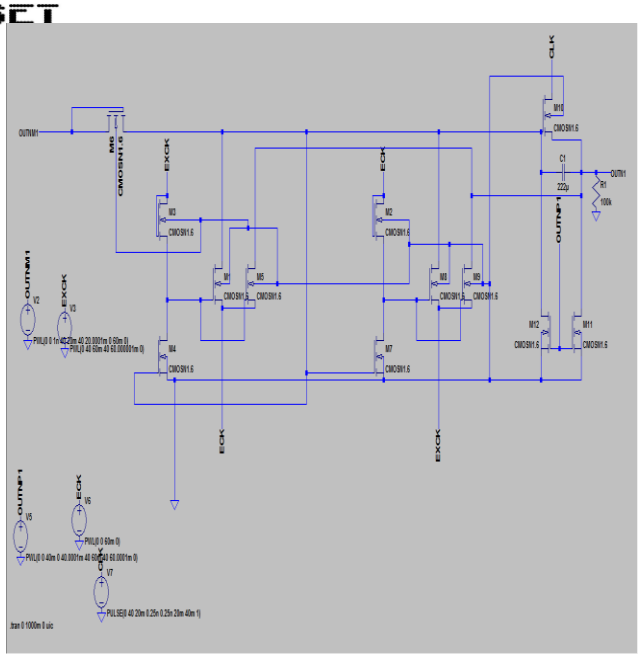

Fig1 (a) Schematic diagram

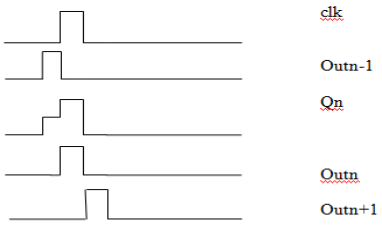

Fig1 (b) Timing diagram

Fig.1 (a) illustrated proposed gate driver circuit & Fig.1 (b) Shows timing diagram. It use three clocks one driving clock, two extended clock which shows clock modification. For applying reversed bias stress mechanism it use one pull up network, one key pull down network & two alternative pull down network. As shows in fig.1 high input signal apply at outn-1 when clk1 is in low state & Qn node become high, in the next stage clk1 switches from low to high & Qn node is boosted up due to capacitive gate source coupling[10] at this time out n becomes high through pull up transistor for row lines. In the next stage Qn & Outn node discharge through pull down TFTs and outn+1 becomes high. Hence results are verify that proposed gate driver circuit better than other gate driver circuit because it's stably operate for 360h at high temperature and power consumption also reduced via clock modification, using reversed bias stress.

Table1.

Design Parameter	Reference paper [6]	Reference paper [9]	Reference paper [10]
Voltage swing of gate driver circuit	40v(-10v~30v) to 10v (-10v~0v)	38.4v	39.2v
Lifetime	10minutes	>10 days	>15 days
Test Temperature	100^0C	100^0C	120^0C

III. Conclusion

This paper presents brief study on working of Gate Driver Circuit for TFT-LCD and it gives different techniques for future research scholar to choose good technique as per his/her requirement. But the novel low power gate driver circuit using a-Si:H is a better technique in respect of power consumption, threshold voltage shift & stable output during long operation.

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