

# PFC Based DC Variable Voltage Converter Fed BLDC Motor Drive

R.S.Jothilakshmi<sup>1</sup>, Dr.I.Gerald Christopher Raj<sup>2</sup>, Dr. S.K.Nandhakumar<sup>3</sup>

Department of EEE, PSNA College of Engineering and Technology, Dindigul, Tamilnadu, India<sup>1,2,3</sup>

**ABSTRACT:** This paper presents a power factor corrected (PFC) variable DC converter fed brushless dc motor (BLDCM) drive as a cost effective solution for low-power household applications. The variable DC converter operation is based on canonical switching cell (CSC) topology. The speed of BLDCM is controlled by varying the dc-bus voltage of voltage source inverter (VSI). The BLDCM is electronically commutated for reduced switching losses in VSI due to low-frequency switching. A front-end CSC converter operating in discontinuous inductor current mode (DICM) is used for dc-bus voltage control with unity power factor at ac mains. A single sensor for dc-bus voltage sensing is used for the development of the proposed drive, which makes it a cost-effective solution. The performance of the proposed drive is evaluated over a wide range of speed control and variable loading conditions with improved power quality at ac mains. The performance of the proposed drive is simulated in MATLAB/Simulink environment.

**KEYWORDS:** Brushless dc motor, canonical switching cell converter, discontinuous inductor current mode, power factor correction, power quality.

## I.INTRODUCTION

Among numerous motors, brushless dc motor (BLDCM) is favorite in many low and medium power applications including household appliances, industrial tools, heating ventilation and air conditioning (HVAC), medical equipment, and precise motion control systems [1]–[7]. BLDCM is preferred because of its high torque/inertia ratio, high efficiency, ruggedness, and low-electro-magnetic interference (EMI) problems [1], [2]. The stator of the BLDCM comprises of three-phase concentrated windings and rotor has permanent magnets [1], [2]. It is also recognized as an electronically commutated motor (ECM) since an electronic commutation created on rotor position via a three-phase voltage source inverter (VSI) is used [8], [9]. Thus, the problems associated with brushes, such as sparking, and wear and tear of the commutator assembly are excluded. Fig. 1 shows a conventional arrangement of BLDCM drive fed by an uncontrolled rectifier and a dc-link capacitor followed by a three-phase VSI, which is based on pulse width modulation (PWM) is used for feeding the BLDCM [10]. This type of arrangement draws peaky, harmonic rich current from the supply

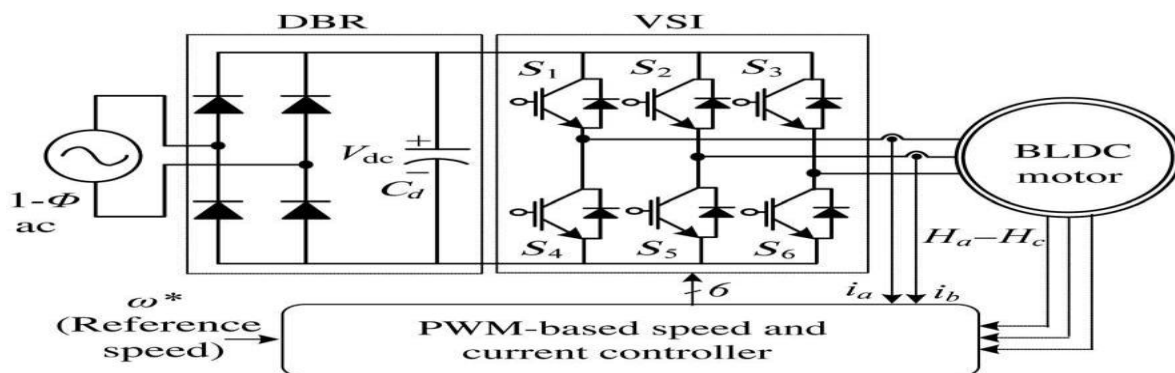


Fig. 1. Conventional BLDCM drive

and leads to a high value of total harmonic distortion (THD) of supply current and very low power factor at its supply mains. A very high THD of supply current of 65.3% and a very poor power factor of 0.72 is realized.

A front-end power factor correction (PFC) converter is used after the diode bridge rectifier (DBR) for refining the quality of power and attaining a near unity power factor at ac supply mains. The continuous inductor current mode (CICM) and the dis-continuous inductor current mode (DICM) are the two basic modes of operation of a PFC converter. A control of current multiplier is normally used for PFC converter operating in CICM and requires three sensors (2-V, 1-C) for the operation which is not cost-effective for low-power applications, whereas, a PFC converter operating in DICM uses a voltage follower control which requires sensing of dc-link voltage for voltage control and natural PFC is attained at ac mains [13], [14].

Many topologies of a PFC-based BLDCM drives have been stated in the literature [10], [15]–[23]. A boost PFC converter has been the most popular arrangement for feeding BLDCM drive as shown in Fig. 2 [16]–[18]. A constant dc-link voltage is conserved at the dc-link capacitor and a PWM-based VSI is used for the speed control. Hence, the switching losses in VSI are very high due to high switching PWM signals and require huge quantity of sensing for its operation. Cheng [19] has proposed an active rectifier-based BLDC motor drive fed which requires complex control and is suitable for higher power applications.

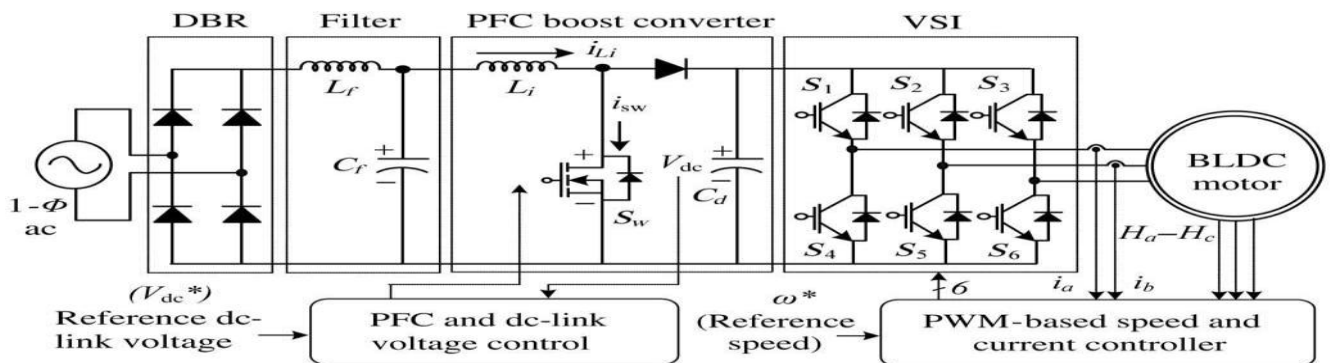


Fig.2. Conventional BLDCM drive with PFC converter

Lee et al. [20] have discovered numerous reduced parts formations for PFC operation which also uses a PWM-based VSI and have high switching losses in it. A buck chopper operating as a front-end converter for feeding a BLDC motor drive has been projected by Barkley et al. [21]. It also has greater switching losses associated with it due to high-frequency switching. Madani et al. [22] have suggested a boost half bridge PFC-based BLDCM drive using four switch VSI. This also needs an essential PWM operation of VSI and PFC half bridge boost converter, which presents high switching losses in the whole system.

These switching losses are condensed by using an idea of variable dc-link voltage for speed control of BLDC motor [24]. This exploits the VSI to operate in low-frequency switching mandatory for electronic commutation of BLDC motor, therefore condenses the switching losses related with it. The front-end SEPIC and Cuk converter serving a BLDC motor using a variable voltage control have been offered in [10] and [23], but at the cost of two current sensors. This paper presents the development of a reduced sensor-based BLDC motor drive for low-power application.

## II. PROPOSED DRIVE USING IMPROVED DC CONVERTER

Fig. 3 shows the proposed BLDCM drive with improved dc converter which includes a front-end PFC-based canonical switching cell (CSC) converter. A CSC converter working in DICM acts as an inherent power factor pre-regulator for attaining a unity power factor at ac mains.

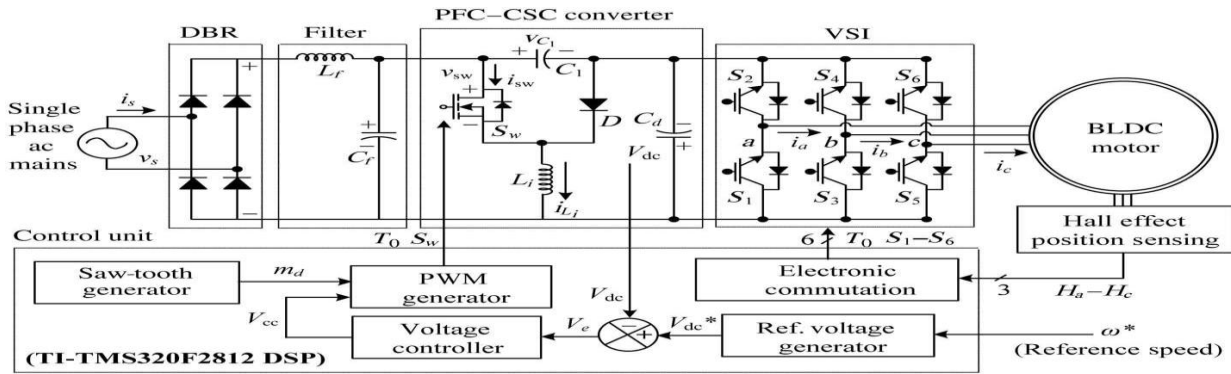


Fig.3. Proposed BLDCM drive fed from CSC converter

An adjustable dc-bus voltage of the VSI is used for controlling the speed of the BLDCM. This operates the VSI in low-frequency switching by electronically commutating the BLDCM for reducing the switching losses in six insulated gate bipolar transistor's (IGBT's) of VSI which share the major portion of total losses in the BLDCM drive. The front-end CSC converter is designed and its parameters are selected to operate in a DICM for obtaining a high-power factor at wide range of speed control.

### III. OPERATING PRINCIPLE OF PROPOSED DC CONVERTER

The proposed BLDCM drive uses a CSC converter working in DICM [25]–[28]. In DICM, the current in inductor  $L_i$  becomes discontinuous in a switching period ( $T_s$ ). Three states of CSC converter are shown in Fig. 4(a)–(c). Three modes of operation are described as follows.

**Mode I:** As shown in Fig. 4(a), when switch  $S_w$  is turned ON, the energy from the supply and stored energy in the intermediate capacitor  $C_1$  are moved to inductor  $L_i$ . In this process, the voltage across the intermediate capacitor  $V_{C1}$  reduces, while inductor current  $i_{Li}$  and dc-link voltage  $V_{dc}$  are augmented. The designed value of intermediate capacitor is large enough to hold enough energy such that the voltage across it does not become discontinuous.

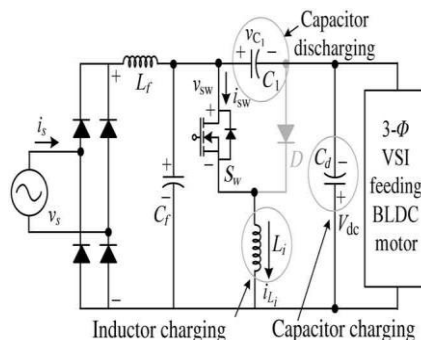


Fig.4 (a). Operation of CSC converter in Mode I

**Mode II:** The switch is turned OFF in this mode of operation as shown in Fig. 4(b). The intermediate capacitor  $C_1$  is charged through the supply current whereas inductor  $L_i$  starts discharging hence voltage  $V_{C1}$  starts growing, while current  $i_{Li}$  falls in this mode of operation. Furthermore, the voltage across the dc-link capacitor  $V_{dc}$  continues to rise due to discharging of inductor  $L_i$ .

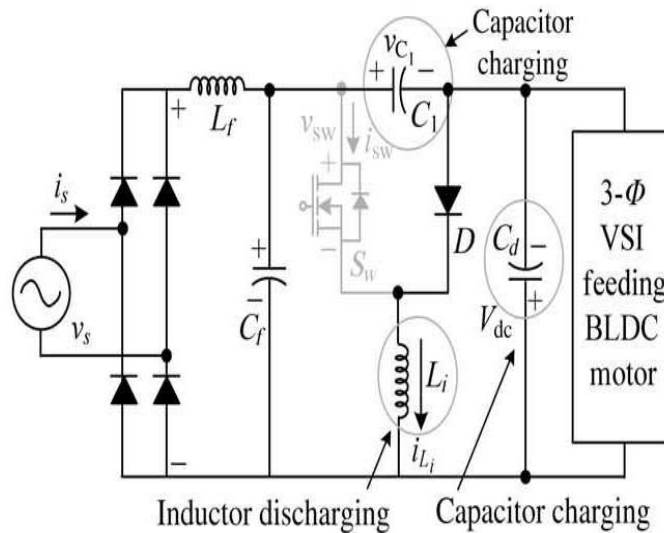


Fig.4 (b).Operation of CSC converter in Mode II

Mode III: This is the discontinuous conduction mode of operation as inductor  $L_i$  is entirely discharged and current  $i_{L_i}$  becomes zero as shown in Fig. 4(c). The voltage across intermediate capacitor  $C_1$  remains to increase, while dc-link capacitor supplies the essential energy to the load, hence  $V_{dc}$  starts falling.

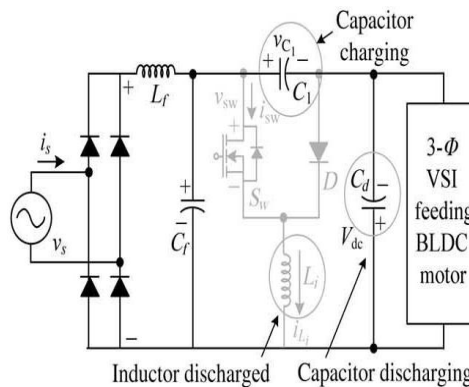


Fig.4 (c).Operation of CSC converter in Mode III

**IV.DESIGN OF IMPROVED VARIABLE DC CONVERTER**

The proposed BLDCM drive uses a PFC-based CSC converter operating in DICM. The voltage appearing after the DBR is given as

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} \dots\dots\dots(1)$$

A nominal duty ratio ( $d_n$ ) corresponding to  $V_{dcn}$  is as

$$d_n = \frac{V_{dcn}}{V_{dcn} + V_{in}} \dots\dots\dots(2)$$

The design of a CSC converter is very similar to a non-isolated Cuk converter with a single inductor and a switching

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cell which is a combination of a switch  $S_w$ , diode  $D$ , and an intermediate capacitor  $C_1$  [14]. The critical value of inductance  $L_{ic}$  to operate at boundary condition is given as

$$L_{ic} = \frac{V_{in} d_{nom}}{2I_{in} f_s} \dots\dots\dots(3)$$

Where  $I_{in}$  is inductor, ( $L_i$ ) current, and  $f_s$  is switching frequency. Now to operate this converter for PFC even at very low duty ratio, the value of inductor is taken around 1/10 th of the critical value [29]. Hence, it is

$$L_i = \frac{L_{ic}}{10} \dots\dots\dots(4)$$

An intermediate capacitor  $C_1$  is designed for permitted ripple voltage of  $\Delta V_{C1}$  across it and it is taken as 10% of  $V_C$ , where  $V_C$  is the voltage across intermediate capacitor

$$C_1 = \frac{V_{dcnom} d_{nom}}{f_s R_L \Delta V_{C1}} \dots\dots\dots(5)$$

Where  $R_L$  is the equivalent emulated load resistance. Now for a permitted ripple of 1% of the nominal dc-link voltage across the dc-link capacitor ( $C_d$ ), the value of dc-link capacitor is calculated as

$$C_d = \frac{I_d}{2\omega_L \Delta V_{dc}} \dots\dots\dots(6)$$

where  $\omega_L$  is line frequency in rad/s and  $I_d$  is dc-link current.

To avoid the reflection of high-order harmonics in supply system, a low-pass inductive-capacitive (LC) filter is designed

whose maximum value,  $C_{max}$  is calculated as

$$C_{max} = \frac{I_{peak}}{\omega_L V_{peak}} \tan(\theta) \dots\dots\dots(7)$$

Where  $I_{peak}$  and  $V_{peak}$  are amplitudes of supply current and supply voltage and  $\theta$  is the displacement angle between them. Now, the value of filter inductor is designed by considering the source impedance ( $L_s$ ) of 4%–5% of the base impedance. Hence, the additional value of inductance required is given as

$$L_f = L_{req} + L_s \rightarrow \frac{1}{4\pi^2 f_c^2 C_f} \dots\dots\dots(8)$$

**V. SIMULATION MODEL OF IMPROVED VARIABLE DC CONVERTER FED BLDCM DRIVE**

The control of the proposed drive is classified into control of DC converter and BLDCM. The improved DC converter operating in DICM is organized via a control of voltage follower. It produces PWM pulses for maintaining the required dc-link voltage at the input of VSI. A single-voltage sensor is used for the control of the improved DC converter operating in DICM. The control of BLDCM is accomplished with an electronic commutation, which includes proper switching of VSI in such a way that a symmetrical dc current is drawn from the dc-link capacitor for 120° and placed symmetrically at the centre of back electro-motive force (EMF) of each phase. A Hall-Effect position sensor is used to sense the rotor position on a span of 60°, which is required for the electronic commutation of BLDCM. The Simulation model of the proposed drive is shown in fig. 5.

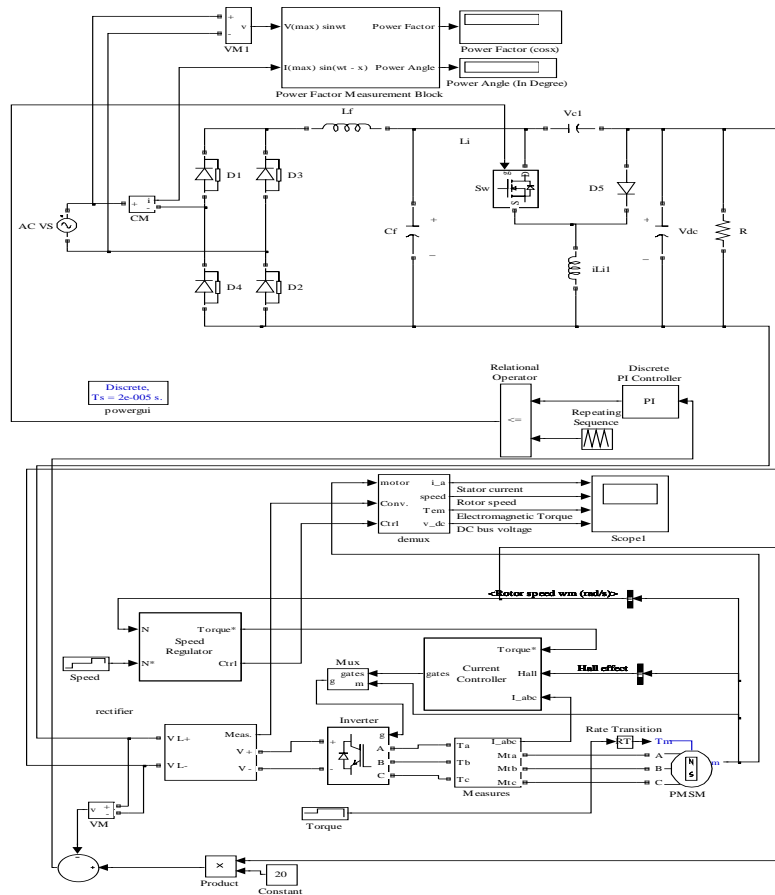


Fig. 5. Simulink Model of proposed BLDCM drive fed from improved variable DC converter

### VI. SIMULATED PERFORMANCE OF PROPOSED BLDCM DRIVE

The performance of the proposed BLDCM drive is simulated in MATLAB/Simulink environment using the Sim-

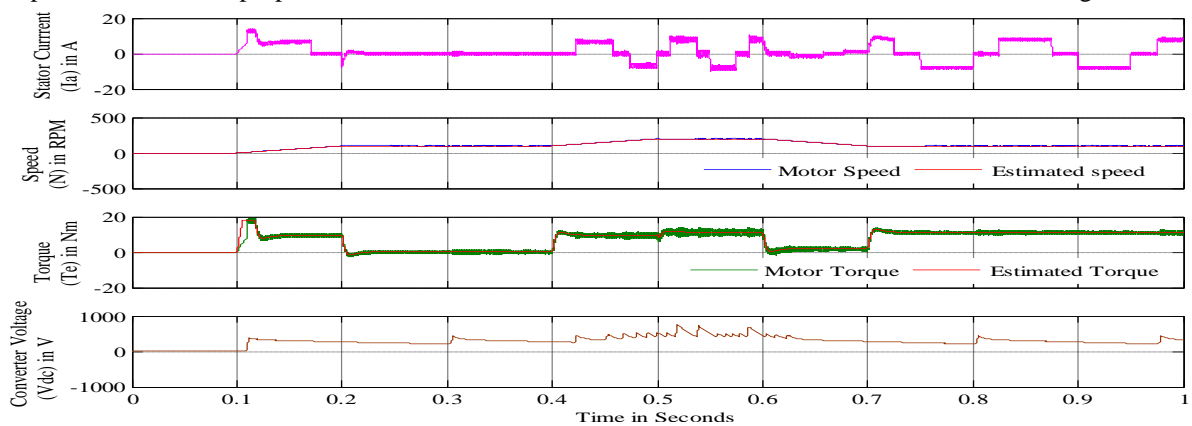


Fig. 6. Dynamic performance of proposed BLDCM drive during speed and torque command variations



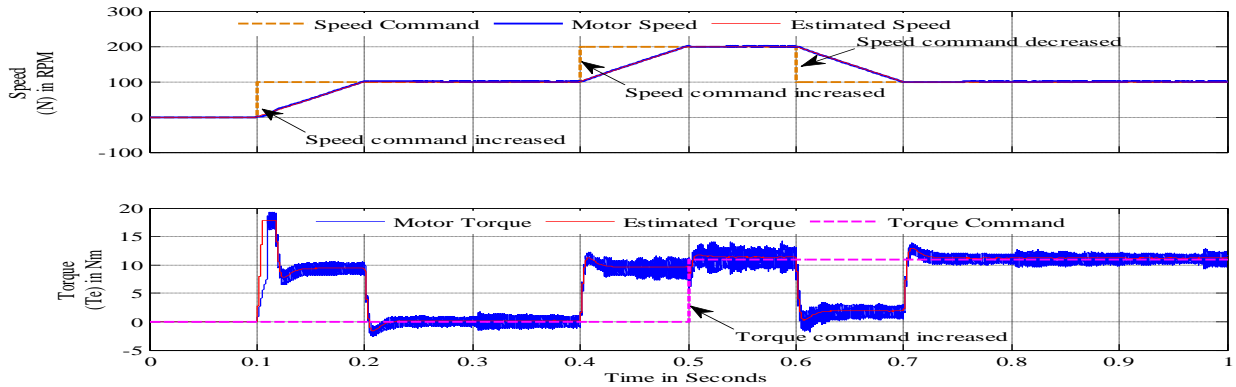


Fig. 7. Dynamic performance of proposed BLDCM drive during speed and torque command variations along with estimated speed and torque

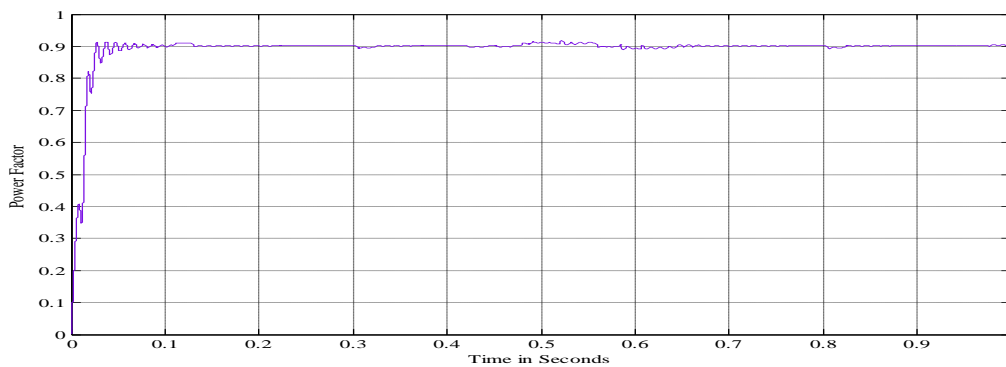


Fig.8. Variation of PF during speed and torque command variations

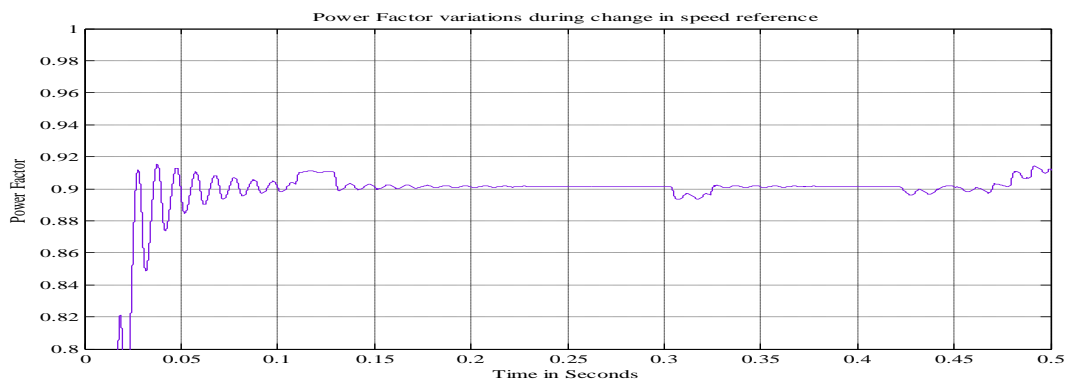


Fig.9. Variation of PF during speed command variation at 0.5 seconds

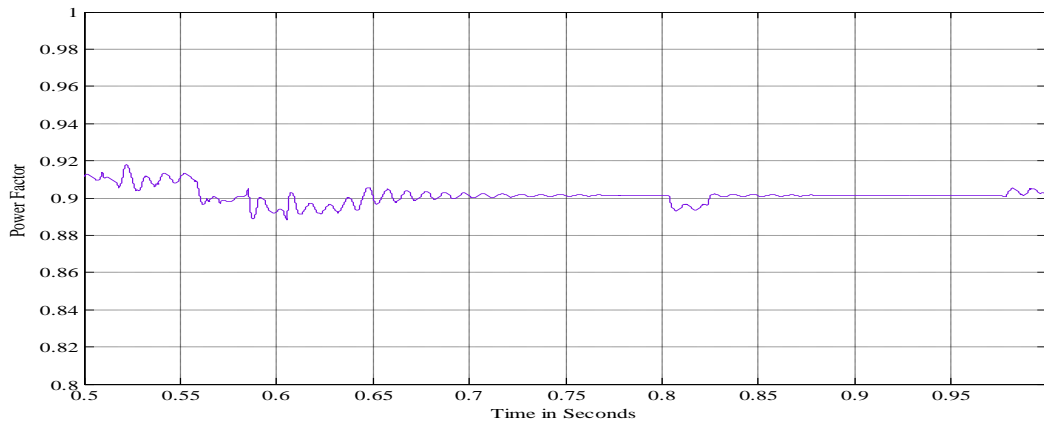


Fig.10.Variation of PF during torque command variation at 0.5 seconds

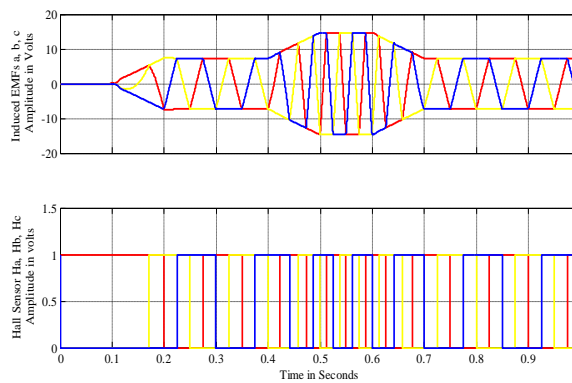


Fig.11.Induced EMFs and Hall Position Sensing under transient conditions of proposed BLDCM drive

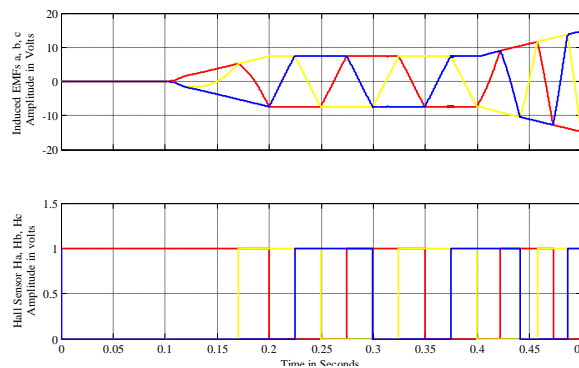


Fig. 12.Induced EMFs and Hall Position Sensing under transient conditions of proposed BLDCM drive



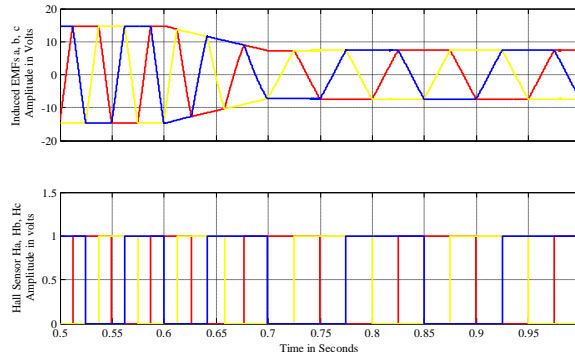


Fig. 13. Induced EMFs and Hall Position Sensing under transient conditions of proposed BLDCM drive

Power-System toolbox. The simulation parameters are listed in table I. The performance evaluation of the proposed drive is categorized in terms of the performance of the BLDC motor and improved variable DC converter and the achieved power quality indices obtained at ac mains. The parameters associated with the BLDC motor such as speed ( $N$ ), electromagnetic torque ( $T_e$ ), and stator current ( $i_a$ ) are analyzed for the proper functioning of the BLDC motor. Parameters such as supply voltage ( $V_s$ ), supply current ( $i_s$ ), dc link voltage ( $V_{dc}$ ), of improved DC converter are evaluated to demonstrate its proper functioning. Moreover, power quality indices such as power factor (PF) total harmonic distortion (THD) are analyzed for determining power quality at ac mains.

## VII. CONCLUSION

PFC Based DC Variable Voltage Converter fed BLDC drive has been proposed for targeting low-power domestic applications. Anadjustable voltage of dc bus has been used for controlling the speed of BLDCM which ultimately has given the freedom to operate VSI in low-frequency switching mode for reduced switching losses. A front-end CSC converter operating in DICM has been used for dual objectives of dc-link voltage control and realizing almost unity power factor at ac mains. The performance of the proposed drive has been found quite well for its operation at variation of speed over a wide range and also variable loading conditions. A prototype of the CSC-based BLDCM drive has to beimplementing with satisfactory test results for its operation over complete speed range and its operation at universal ac mains in future.

TABLE I  
SIMULATION PARAMETERS

Symbol	Quantity	Parameter
$V_s$	Supply Voltage	200 V, 50Hz
$V_{dcn}$	Nominal Voltage	120V
$L_f$	Filter Inductance	3.77mH
$C_f$	Filter Capacitance	330nF
$iLi1$	Initial Current Inductance	924.75 $\mu$ H
$R$	Resistance	100 $\Omega$
$V_{C1}$	Intermediate Capacitance	494.49nF
$V_{dc}$	Capacitance (DC Link Voltage)	2211.6 $\mu$ F
$R_s$	Stator resistance	0.2 ohms
$L_s$	Stator inductance	8.5 mH

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$p$	Number of poles	4
$P$	Rated power	314.16 w
$V_{dc}$	Rated dc bus voltage	220v
$N$	Rated speed	200 rpm
$C_f$	Filter Capacitance	330nF
$iLi1$	Initial Current Inductance	924.75 $\mu$ H
$R$	Resistance	100 $\Omega$
$V_{C1}$	Intermediate Capacitance	494.49nF

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