

- 'ALS679 is a 12-Bit Address Comparator with Enable
- 'ALS680 is a 12-Bit Address Comparator with Latch
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

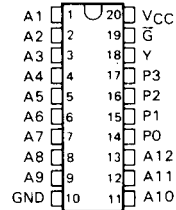
**description**

The 'ALS679 and 'ALS680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

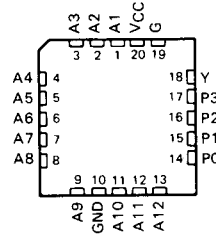
The 'ALS679 features an enable input ( $\bar{G}$ ). When  $\bar{G}$  is low, the device is enabled. When  $\bar{G}$  is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

The SN54ALS679 and SN54ALS680 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS679 and SN74ALS680 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

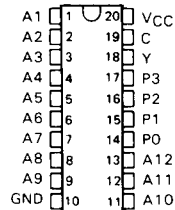
**SN54ALS679 . . . J PACKAGE  
SN74ALS679 . . . DW OR N PACKAGE  
(TOP VIEW)**



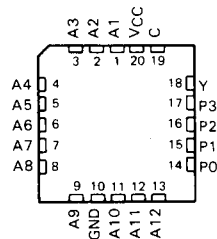
**SN54ALS679 . . . FK PACKAGE  
(TOP VIEW)**



**SN54ALS680 . . . J PACKAGE  
SN74ALS680 . . . DW OR N PACKAGE  
(TOP VIEW)**



**SN54ALS680 . . . FK PACKAGE  
(TOP VIEW)**



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# SN54ALS679, SN54ALS680, SN74ALS679, SN74ALS680

## 12-BIT ADDRESS COMPARATORS

FUNCTION TABLE

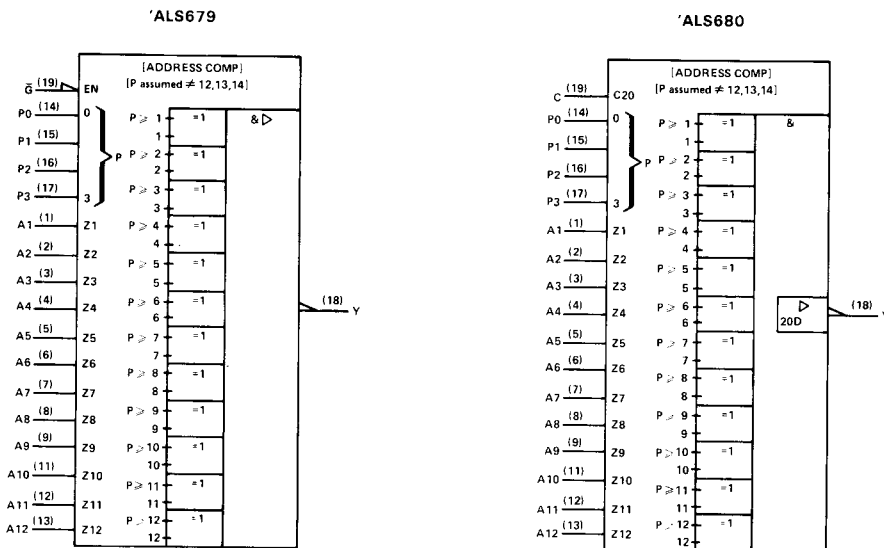
'ALS679 $\bar{G}$	'ALS680 C	INPUTS COMMON TO 'ALS679 AND 'ALS680											OUTPUT Y					
		P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7		A8	A9	A10	A11	A12
L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	H	L	L	L	L	L	L	L	H	H	H	L	L†
L	H	L	H	H	L	H	L	L	L	L	L	L	L	L	H	H	L	L†
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	L	L†
L	H	All other combinations															H	
H	'ALS679: Any combination																H	
L	L	'ALS680: Any combination															Latched	

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†The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which  $P = 12, 13, \text{ and } 14$ . If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change  $P \geq 9$  to  $P = 9 \dots 11/13 \dots 15, P \geq 10$  to  $P = 10/11/14/15$ , and  $P \geq 11$  to  $P = 11/15$ .

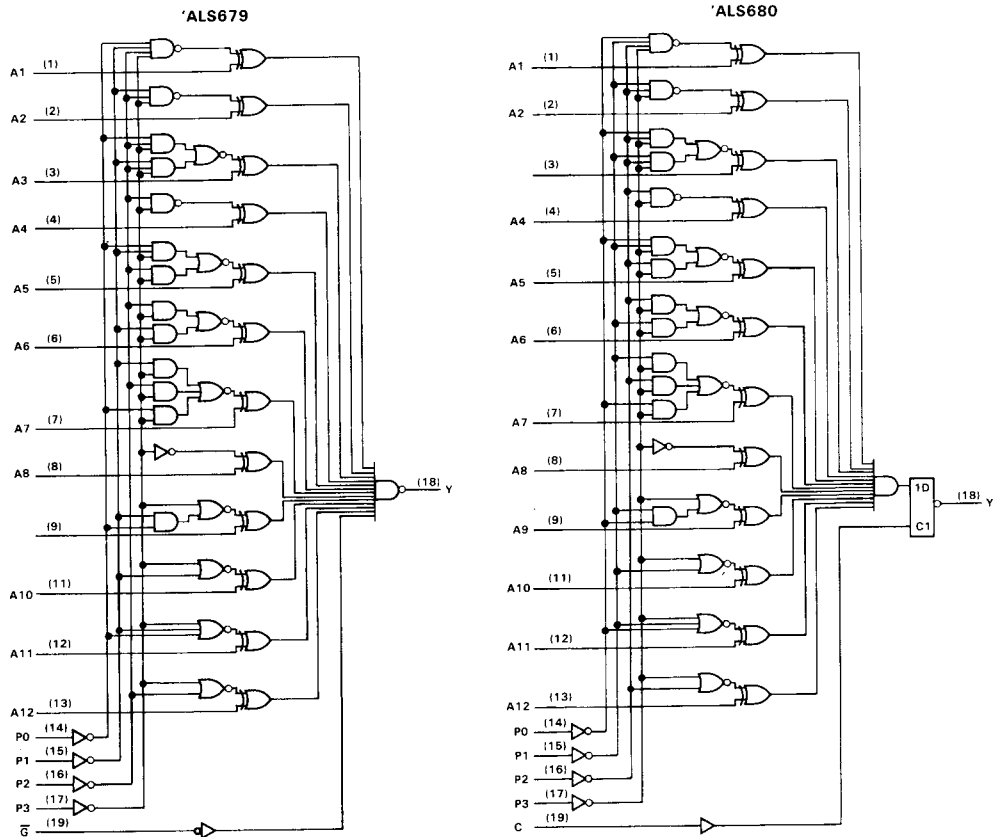
logic symbols‡



‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS679, SN54ALS680, SN74ALS679, SN74ALS680  
12-BIT ADDRESS COMPARATORS

logic diagrams (positive logic)



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**SN54ALS679, SN54ALS680, SN74ALS679, SN74ALS680**  
**12-BIT ADDRESS COMPARATORS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ .....	7 V
Input voltage .....	7 V
Operating free-air temperature range: SN54ALS679, SN54ALS680 .....	-55°C to 125°C
SN74ALS679, SN74ALS680 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

recommended operating conditions

		SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
$V_{IH}$	High-level input voltage	2			2			V		
$V_{IL}$	Low-level input voltage	0.7			0.8			V		
$I_{OH}$	High-level output current	-1			-2.6			mA		
$I_{OL}$	Low-level output current	12			24			mA		
$t_w$	Pulse duration, Enable C high	'ALS680			40			ns		
$t_{su}$	Setup time, Data before C↓	'ALS680			45			ns		
$t_h$	Hold time, Data after C↓	'ALS680			5			ns		
$T_A$	Operating free-air temperature	-55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	
$V_{IK}$	$V_{CC} = 4.5 V, I_I = -18 mA$	-1.5			-1.5			V
$V_{OH}$	$V_{CC} = 4.5 V \text{ to } 5.5 V, I_{OH} = -0.4 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 V, I_{OH} = -1 mA$	2.4			3.3			
	$V_{CC} = 4.5 V, I_{OH} = -2.6 mA$	2.4			3.2			
$V_{OL}$	$V_{CC} = 4.5 V, I_{OL} = 12 mA$	0.25			0.4			V
	$V_{CC} = 4.5 V, I_{OL} = 24 mA$	0.25			0.5			
$I_I$	$V_{CC} = 5.5 V, V_I = 7 V$	0.1			0.1			mA
$I_{IH}$	$V_{CC} = 5.5 V, V_I = 2.7 V$	20			20			μA
$I_{IL}$	$V_{CC} = 5.5 V, V_I = 0.4 V$	-0.1			-0.1			mA
$I_{O}^{\ddagger}$	$V_{CC} = 5.5 V, V_O = 2.25 V$	-30			-112			mA
$I_{CC}$	'ALS679	17			27			mA
	'ALS680	18			27			

<sup>†</sup>All typical values are at  $V_{CC} = 5 V, T_A = 25^\circ C$ .

<sup>‡</sup>The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

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**SN54ALS679, SN54ALS680, SN74ALS679, SN74ALS680**  
**12-BIT ADDRESS COMPARATORS**

**'ALS679 switching characteristics (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS679		SN74ALS679		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	Any P	Y	4	28	4	25	ns
$t_{PHL}$			8	40	8	35	
$t_{PLH}$	Any A	Y	5	26	5	22	ns
$t_{PHL}$			5	35	5	30	
$t_{PLH}$	$\bar{G}$	Y	3	15	3	13	ns
$t_{PHL}$			5	30	5	25	

**'ALS680 switching characteristics (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS680		SN74ALS680		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	Any P	Y	6	27	6	22	ns
$t_{PHL}$			10	43	10	38	ns
$t_{PLH}$	Any A	Y	5	25	5	21	ns
$t_{PHL}$			5	28	5	25	
$t_{PLH}$	C	Y	3	25	3	20	ns
$t_{PHL}$			15	48	15	42	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

# SN54ALS679, SN54ALS680, SN74ALS679, SN74ALS680 12-BIT ADDRESS COMPARATORS

## TYPICAL APPLICATION INFORMATION

The 'ALS679 and 'ALS680 can be wired to recognize any one of  $2^{12}$  addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made:

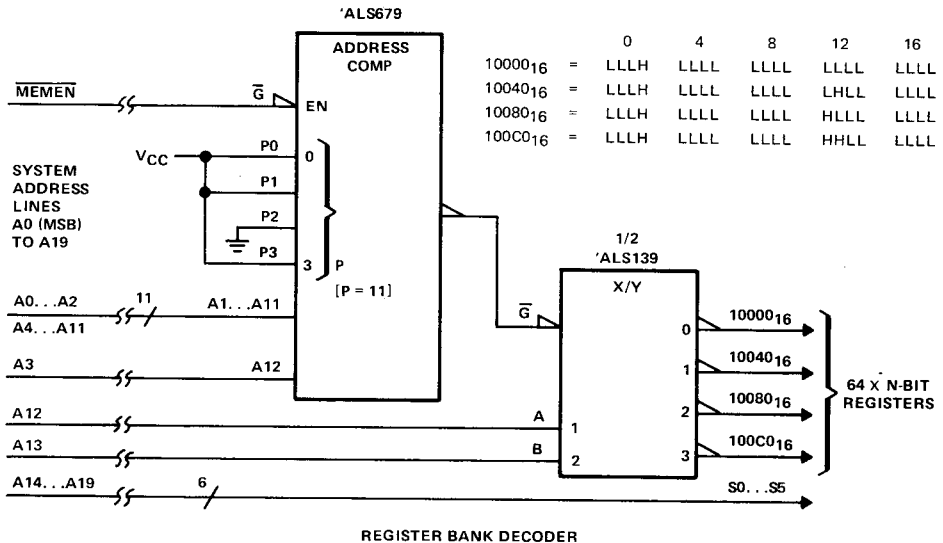
P3 to 0 V, P2 to VCC, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.



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