Product Bulletin

Texas Instruments Gen 2 Integrated Circuit:

Gen 2 IC Based on EPCglobal Gen 2 Specification

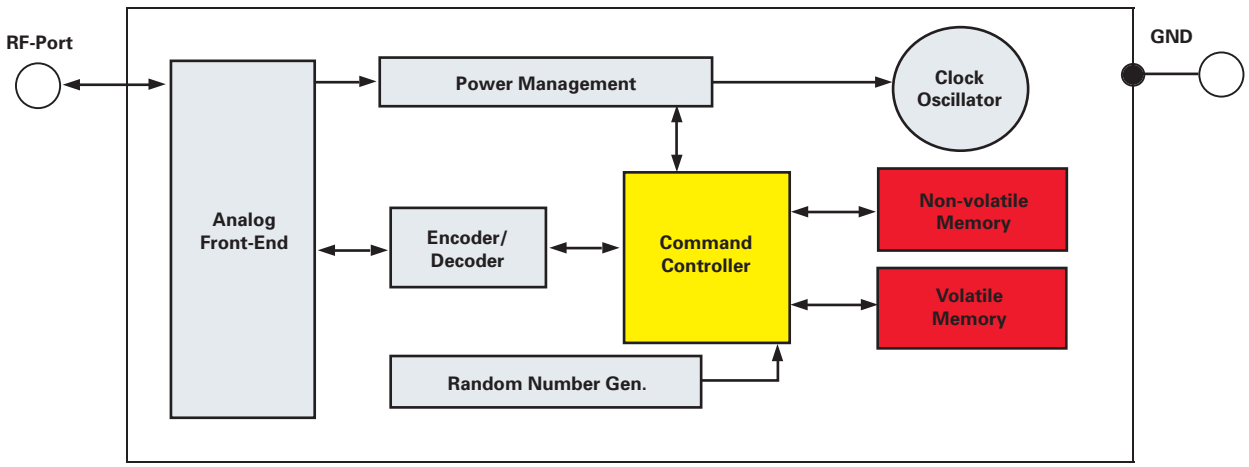
Key Features

- Meets EPCglobal Gen 2 (v. 1.0.9) and ISO/IEC 18000-6c
- Global frequency operability, 860-960 MHz
- Supports optional Gen 2 commands: Block Write and Block Erase
- 192-bit memory: 96-bit EPC, 32-bit access password, 32-bit kill password, 32-bit TID memory
- Designed for high-performance, low power consumption based on the most advanced silicon process node for RFID (130 nm)
- Fast tag singulation using the most advanced anti-collision scheme
- Suitable for E-field and H-field applications
- RoHS compliant

Since 1989, Texas Instruments has been manufacturing ICs for a wide array of RFID applications. This heritage has provided TI with strong expertise in the design of ICs used in RFID, and the high quality manufacturing and testing techniques developed over the years have separated TI from the competition. Being a global leader in integrated circuit design and fabrication allows TI to leverage its core strengths and deliver a UHF Gen 2 chip built on the company's 130 nm process node.

The Gen 2 chip is intended for use in the manufacture of passive RFID tag products operating in the 860 to 960 MHz frequency band. Meeting all of the EPCglobal Gen 2 and ISO/IEC 18000-6c required specifications with 192 bits of memory, this chip also goes beyond the standard requirements to provide additional functionality by supporting "block write" and "block erase" commands. This important feature provides faster data communication between the tag and the reader/interrogator. In addition, the chip incorporates a Shottky diode that provides increased tag sensitivity, allowing for longer read range and a more reliable read/write exchange between the tag and the reader.

While primarily intended for the supply chain market, the Gen 2 chip may also be used in asset tracking, baggage tagging, manufacturing, and a wide assortment of other applications where long read range is required. The chip is available in raw wafer form, or bumped, back ground, and sawn. A wafer map is also provided.



Simplified block diagram.

Specification Table

Protocol	EPCglobal Gen 2 specification (V 1.0.9)
Frequency	860 – 960 MHz
Communication Mode	Half Duplex, Reader talks first
Data rate	Uplink: 40 to 640 Kbps, Downlink: 40 to 160 Kbps
Modulation	Downlink: ASK or PR-ASK, Uplink: ASK
Operating Temperature	–40°C to + 65°C (Read), –25°C to +65°C (Write)
Chips Per Wafer	> 40,000
Commands Supported	EPCglobal Class 1 Gen 2 and ISO/IEC 18000-6c mandatory commands, optional block write and erase
Encoding	Uplink: FM0, Miller, Downlink: PIE
Read Range	7.0 m, (6.6 m in Europe) typical*

** Read range distance is for reference only. Actual read range distance may vary according to tagged materials, antenna design, reader, and environmental circumstances. Maximum tag write distance is typically 70% of read distance.*

Wafer Ordering Information

Part Number	Bumped	Backgrind	Sawn	Wafer Map	Wafer size
RI-UHF-11111-01	Yes	Yes	Yes	Yes	8" (200 mm)
RI-UHF-00001-01	No	No	No	Yes	8" (200 mm)

For more detailed information, please visit the document center at www.ti.com/rfid. The EPC Gen 2 integrated circuit is also available in a "Strap" form factor (part # RI-UHF-STRAP-08).

Additional information on the strap version and all of the RFID products from Texas Instruments is available on our web site.

TI Worldwide Technical Support

Internet

TI RFID Product Information Center Homepage
www.ti.com/rfid

US and Canada Product Information Center
Phone: 800-962-7343

Fax: 214-567-7343

Business Hours (Central Standard Time):
Mon. 8:00 am - 5:00 pm
Tues. 10:00 am - 5:00 pm
Wed. 8:00 am - 5:00 pm
Thurs. 10:00 am - 5:00 pm
Fri. 8:00 am - 5:00 pm

E-mail: rfidsupport@ti.com

Texas Instruments
Radio Frequency Identification Systems
6550 Chase Oaks Blvd., MS 8470
Plano, Texas 75023
USA

European Product Information Center

Country	Phone
Belgium (English)	+32 (0)2 7455455
France (English)	+33 4 93 22 22 00
Germany	+49 (0)8161 80 2200
Italy	+39 (0)39 6568 210
Netherlands (English)	+31 (0)546 879 222
Spain	+34 902 19 73 96
Sweden (English)	+46 (0)8 58755527
UK	+44 (0)1604 88 4088

Fax:
All Languages — +49 (0) 8161 80 2045

Business Hours (Central European Time):
Mon. 8:30 am - 17:30 pm
Tues. 8:30 am - 17:30 pm
Wed. 8:30 am - 17:30 pm
Thurs. 8:30 am - 17:30 pm
Fri. 9:00 am - 16:00 pm

E-mail: e-rfidsupport@ti.com

Texas Instruments
Radio Frequency Identification Systems – European Product Information Center
Deutschland GmbH
Haggertystrasse 1D-85350 Freising
Germany

International Product Information Center
Phone: +1 972-575-4364 (English)

Fax: 214-567-2492

Business Hours (Central Standard Time):
Monday - Friday 8:00 am - 5:00 pm

E-mail: rfidsupport@ti.com

Texas Instruments
Radio Frequency Identification Systems
6550 Chase Oaks Blvd., MS 8470
Plano, Texas 75023
USA

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