1997 2007 SSCS 10th Anniversary

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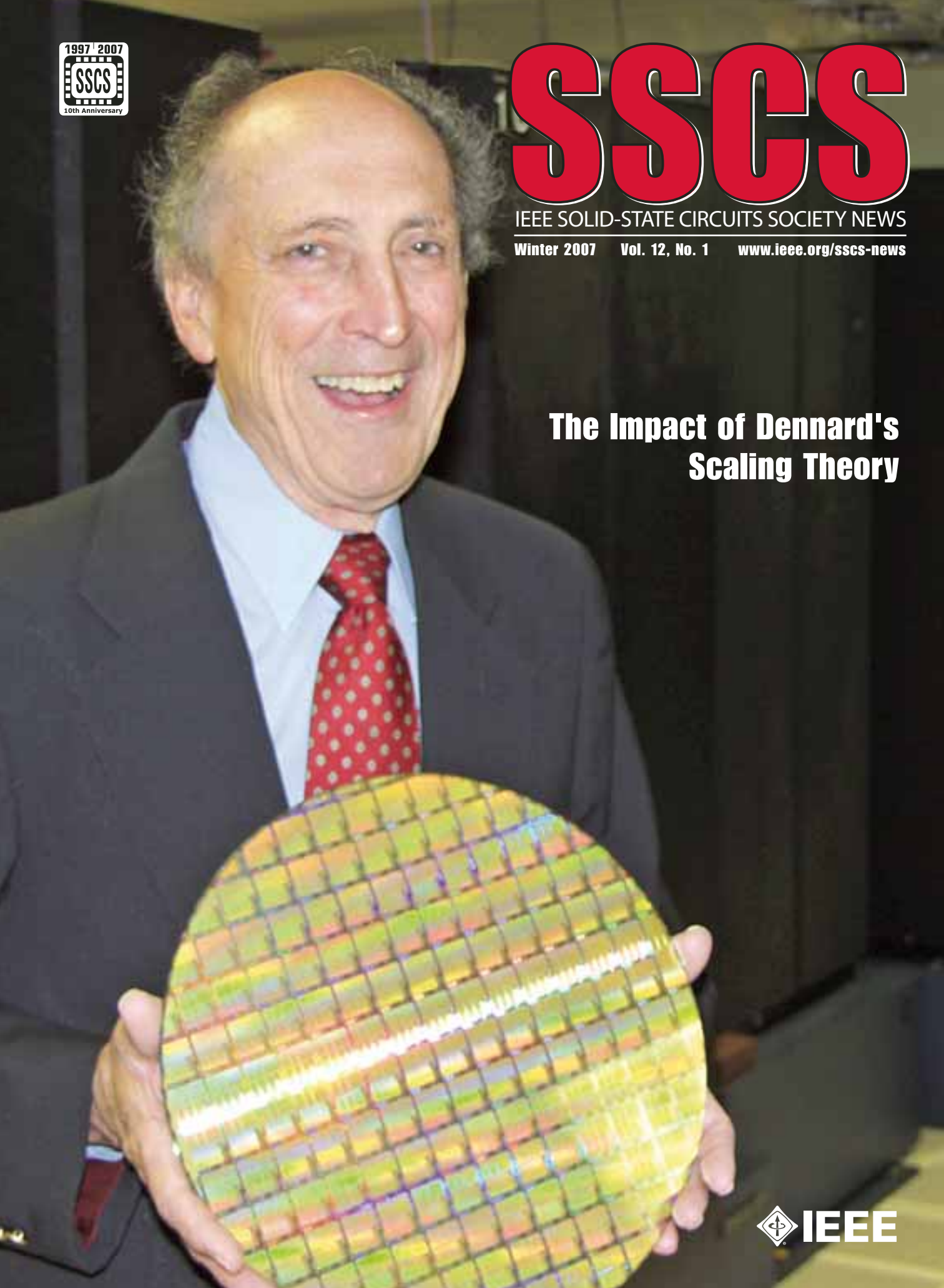

The Impact of Dennard's Scaling Theory

IEEE

Editor's Column

We appreciate all of your feedback on our first issue in September, 2006 on "The Technical Impact of Moore's Law." With the Winter, 2007 issue, we are continuing our new policy of mailing a hard copy of the SSCS News to all 11,500 members. This issue is the first of four that SSCS plans to publish annually (one each in Winter, Spring, Summer, and Fall).

The goal of every issue is to be a self-contained resource on a selected topic, with background articles (that is, the 'original sources') and new articles by experts who describe the current state of affairs in technology and the impact of the original papers and/or patents.

The theme of the Winter 2007 issue is "The Impact of Dennard's Scaling Theory."

This issue contains one Research Highlights article: "Analog IC Design at the University of Twente," by Bram Nauta, Head of the IC Design Group at the University of Twente, The Netherlands. The issue also contains seven short feature articles that address the theme:

(1) "A 30 Year Retrospective on Dennard's MOSFET Scaling Paper," by Mark Bohr of Intel Corporation;
(2) "Device Scaling: The Treadmill that Fueled Three Decades of Semiconductor Industry Growth," by Pallab Chatterjee of i2 Technologies;
(3) "Recollections on MOSFET Scaling," by Dale Critchlow, the University of Vermont;
(4) "The Business of Scaling," by Rakesh Kumar, TCX, Inc. Technology Connexions;
(5) "A Perspective on the Theory of MOSFET Scaling and its Impact," by Tak Ning, IBM;
(6) "Impact of Scaling and the environment in which the Scaling developed

at that time," by Yoshio Nishi, Stanford University;

(7) "It's All About Scale," by Hans Stork, TI.

Three original papers by Dennard, from 1972 (IEDM Conference), 1973 (IEDM Conference), and 1974 (IEEE Journal of Solid-State Circuits), are also reprinted in this issue.

Thank you for taking the time to read the SSCS News. We appreciate your comments and feedback! Please send comments to myl@us.ibm.com.

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Message from the President

In 2007, look for an unadvertised bonus with your SSCS membership: A free subscription to the brand new quarterly Nanotechnology Magazine. We believe that circuit experts need to be in touch with this rapidly progressing technology. Some day it will be a fruitful area for circuits development, and opportunities to contribute will arise.

The minimal subscription cost to the Society for the launch year of the new magazine prompted the AdCom to join the Nanotechnology Council. We hope the Council's magazine effort will be of comparable interest to its Transactions on Nanotechnology, which is just beginning its sixth year and has among the highest rates of citation as measured by the Thompson ISI. I would like to receive feedback from you on how useful a tool the new magazine is. Look for the first issue in the spring of 2007.

2007 is the Society's 10th anniversary, having evolved from the Solid-State Circuits Council that originated in 1970. We've updated the SSCS logo for this year to draw attention to our progress. Since 1997, the Journal of Solid-State Circuits has increased coverage of technical articles by 40%, and the SSCS Newsletter by 2 1/2 times. The JSSC continues to be the most read in IEEE Xplore and the most cited in patents. Your SSCS membership provides online access not only to the Journal but also to the digests of our five major solid-state circuits conferences and most of their historic record. Local chapters have grown from 2 to 59, with the recent addition of Tainan (Taiwan) and South Brazil. Celebrate our anniversary by browsing your technical articles online.

I've been active in the last quarter attending many of the conferences that SSCS cosponsors to sample their quality, focus, and differences, as well as to increase the Society's visibility and support for these important gatherings of technical experts. ESSCIRC in Montreux, Switzerland last fall was fully overlapped with the ESSDERC device conference. One was able to move freely between the co-located meetings. The wide variety of plenary topics covered by the two meetings was of particular interest. Welcoming the Asian-Solid-State Circuits Conference in Hangzhou, China two months later, I was able to talk with circuit experts from around the world, and by the time this issue reaches you, I will have celebrated the opening of the 20th International Conference on VLSI Design in Bangalore.

Thanks to all of our members who voted in our fall election. Welcome to our new additions to AdCom, Kevin Kornegay from Georgia Tech and Harry Lee from MIT. And welcome back to returning AdCom members John Corcoran from Agilent Laboratories, Tom Lee from Stanford, and Jan Van der Spiegel from the University of Pennsylvania. The Society is beginning a review of its priorities for 2007 and beyond. As Society members, please make your interests known to your AdCom representatives. Start a conversation and help the Society point to the future that you feel is coming.

Richard C. Jaeger

Corrections

In the article entitled "Overview of CMOS Technology Development in the MIRAI Project," by Toshiaki Masuhara and Masataka Hirose in the September 2006 issue, the last sentence in the Section entitled "New Circuits and System Technology - Post-fabrication Adaptive Adjustment" contains an incorrect expression, which is corrected as in the underlined expression in the following sentence:

"As shown in Fig. 3, the developed tool successfully extracted the 34 model parameters in 23 hours with a PC and resulted in a mean RMS error of 1.83% <u>for benchmark MOSFETs</u>."

In the Section, "New Gate Stack Technology with High-k Materials", the caption for Figure 4 should read:

Fig. 4 Gate leakage current in MIRAI HfAlON formed by Layer-by-Layer Deposition and Annealing (LL-D&A) [4]).

(a) Comparison of gate leakage current in MOSFETs with HfAlON gate insulator and HfSiON [5]).
(b) Cross sectional TEM micrograph of HfAlON/SiO_2/Si gate stack formed by Layer-by-Layer Deposition and Annealing.

The following corrections pertain to the reprint of "Lithography and the Future of Moore's Law" (Moore, 1995) in the September 2006 issue:

I have reproduced photomicrographs of the first planar transistor and the first commercially-available integrated circuit in Figs 3 & 4. I am particularly fond of the transistor, since it is one of the very few products that I designed myself that actually went into production.

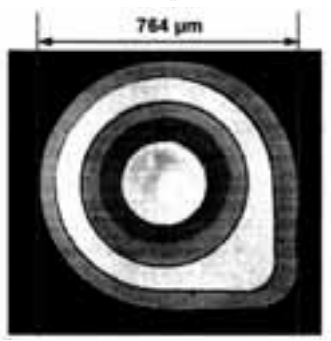

Fig. 3. Photomicrograph of the first commercial planar transistor.

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Analog IC Design at the University of Twente

Bram Nauta, IC Design Group, University of Twente, Enschede, The Netherlands, b.nauta@utwente.nl

Introduction

This article describes some recent research results from the IC Design group of the University of Twente, located in Enschede, The Netherlands.

Our research focuses on *analog* CMOS circuit design with emphasis on high frequency and broadband circuits. With the trend of system integration in mind, we try to develop new circuit techniques that enable the next steps in system integration in nanometer CMOS technology. Our research funding comes from industry, as well as from governmental organizations. We aim to find fundamental solutions for practical problems of integrated circuits realized in industrial Silicon technologies.

CMOS IC technology is dictated by optimal cost and performance of digital circuits and is certainly not optimized for nice analog behavior. As analog designers, we do not have the illusion of being able to change CMOS technology, so we have to "live with it" and solve the problems by design. In this article several examples will be shown where problematic analog behavior, such as noise and distortion, can be tackled with new circuit design techniques. These circuit techniques are developed in such a way that they do benefit from modern technology and thus enable further integration. This way we can improve various analog building blocks for wireless, wire-line and optical communication. Below some examples are given.

Thermal Noise Cancelling

Noise is an important issue; in communication circuits the sensitivity of the receiver is limited by the noise level of the circuits. Especially, the noise of the first amplifier in the receiving chain is of high importance, since after that amplifier the signal is stronger and the allowable noise levels are higher. For narrowband receivers the added noise of the amplifier can be reduced relatively easily. This is done by using resonant structures, built with - for example - integrated spiral inductors and capacitors which provide voltage gain of the narrowband signals and therefore needing less gain from "noisy" transistors. For wideband systems, e.g. for TV tuners, UWB (Ultra Wide Band) communication and future software defined radio, several octaves of bandwidth are needed and simple resonant structures cannot be used. For these applications, low noise gain stages using noisy transistors have to be used, which is quite a challenge. Apart from the gain and noise demands, additional demands, such as input impedance matching and good linearity, need to be satisfied.

Figure 1a shows a wide band first amplifier stage, denoted as a common-source feedback amplifier.

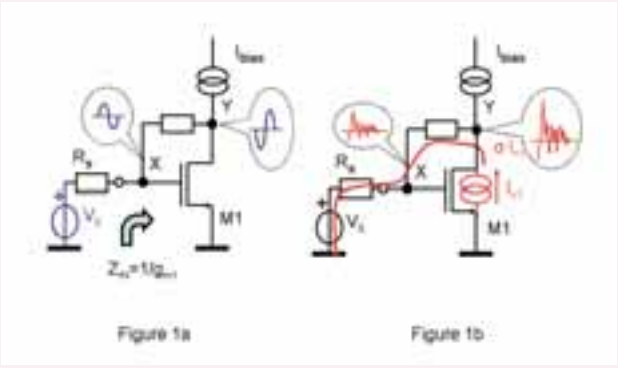

Fig 1a: common source LNA with impedance matching, the signals at nodes X and Y have opposite sign.
Fig 1b: The noise of M1 generates in-phase noise voltages at nodes X and Y.

The input impedance is $1/g_m$ of M1, and must be equal to the source impedance Rs, usually 50 Ohms. With this in mind the gm of M1 is fixed by design resulting in poor noise behavior of the amplifier: The "noise figure" is always larger than 3dB. In order to reduce the noise one would like to increase the g_m of M1 (preferably g_m>>1/Rs for minimal noise figure) but then the input impedance does not match anymore. Conventionally, additional feedback techniques are used to break this paradox, but at the cost of stability and bandwidth issues.

PhD Student Federico Bruccoleri realized, however, that generated noise can be cancelled by proper circuit design. If we take a look at **Figure 1b**, we can see how the noise current of M1 flows in the circuit; this is indicated by the red arrow.

The noise current due to M1 flows in a loop, through Rs. This noise current generates a noise voltage at nodes X and Y which are of different magnitude but of *the same phase*. The signals nodes X and Y are in anti-phase due to the inverting nature of this amplifier. So somehow it should be possible to separate the signal from the noise!

By adding an additional amplifier "A," as shown in **Figure 2**, we can construct an output signal in such a way the wanted signals at nodes X and Y are added and that the noise at nodes X and Y are cancelled [1]. This way we can cancel the noise of M1, which holds for both thermal and 1/f noise. Of course amplifier "A" will now add additional noise, but this needs not to be a problem. The reason for this is that in contrast to M1, we can choose the gm of the input stage of amplifier "A" relatively large, and thus make it low-

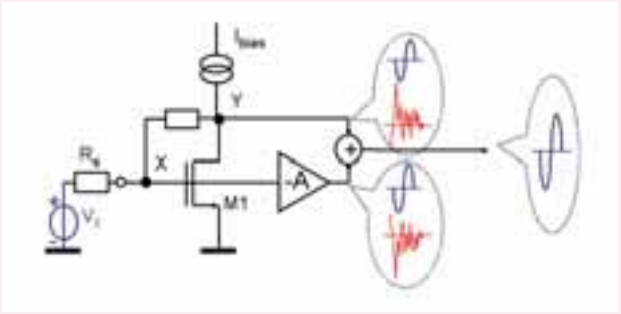

Fig 2: Basic idea of noise cancelling; the noise due to M1 is cancelled.

noise. So we don't break the laws of physics: we still have to burn power (in amplifier "A") to get a low-noise amplifier, but we have created a degree of freedom by decoupling the input matching (g_{m1}=1/Rs) and allowing a large gm (g_{mA}>>1/Rs) in the amplifier A. The noise of I_{bias} is cancelled as well. A prototype amplifier has been realized on silicon and it worked well: the noise figure was well below 3dB, which proves the concept of noise canceling. Also the robustness to mismatch in the two noise paths is good [1]. Other topologies are also possible offering "balun" functionality [1,2].

Low Frequency noise reduction in MOSFETS

Low frequency (LF) transistor noise, also denoted as 1/f noise, is of great importance in today's circuit design. Especially, baseband circuits suffer from this noise phenomenon which can be dominant well above 10MHz. Also high-frequency oscillators suffer from LF noise, since this noise is up-converted and appears close to the carrier frequency of the oscillator degrading the close-in phase noise.

A while ago, a MSc student Gian Hoogzaad did calculations on the phase noise of CMOS inverter-based ring oscillators. These oscillators were free running, and we expected a large close-in phase noise due to the low frequency noise of the MOSFETs in the oscillator. Measurements, however, showed a much lower, (8dB less), close-in phase noise than we expected from the LF noise of those single transistors. The student and his supervisor Sander Gierkink were very confident of his calculations, and we were thus wondering what caused the 8dB lower close-in phase noise.

Finally, we suspected that the large signal switching behavior in the inverters caused the strange effect and we carried out measurements on stand-alone transistors under normal bias and under "switched bias". **Figure 3** illustrates these conditions.

One would expect 6 dB less noise from the switched bias transistors compared to the normal one: 3dB reduction due to the 50% duty-cycle of the noise and another 3dB due to up-conversion of the LF noise.

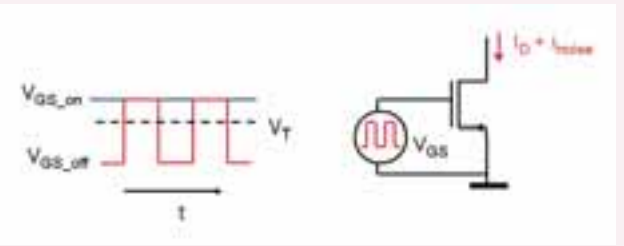

Fig. 3: MOSFET under constant bias (blue) and switched bias (red)

Measurements however showed 6 + 8 = 14 dB reduction for frequencies lower than the switching frequency, as illustrated with the red curve in **Figure 4**.

This matched to the 8dB reduction of phase noise in the inverter ring-oscillator. This reduction takes place for frequencies lower than the switching frequency. Later, we discovered that a similar noise phenomenon had been observed before in physicists' device experiments[3]; however, we could not find a citation to this paper.

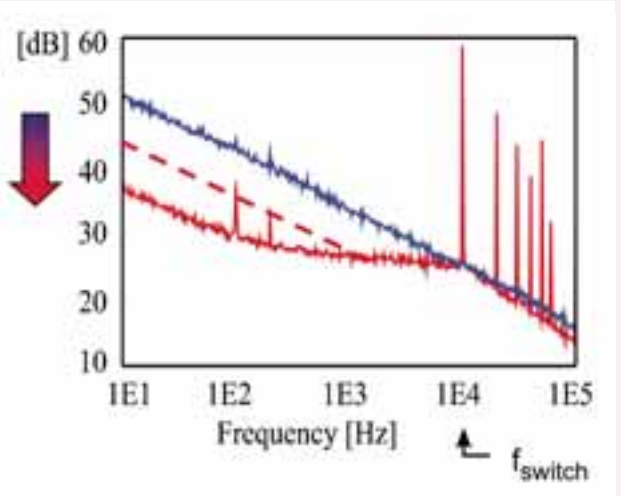

Fig. 4: Measured LF noise of a MOSFET under constant bias (blue), expected 6 dB reduction under switched bias (red dashed curve) and measured behavior with intrinsic reduced noise (red)

So, in fact, all inverter based ring oscillators benefited already from this phenomenon while none of the designers apparently realized this. To a large extent this is because the "switched bias" noise reduction is not modeled in today's simulators. Also, the effect can be masked by the very large spread which is normally present in LF noise, especially for small area devices.

After a study carried out in the PhD projects by Arnoud van der Wel and Jay Kolhatkar, the phenomena could be explained by the bias dependency of the emission and capture time constants which are responsible for the trapping and de-trapping of oxide-charge in MOSFETs. This trapping and de-trapping

causes so-called random telegraph signals, which determine the low frequency noise of the transistors. The reduction effect is found to be present in all technologies investigated: from 10μm down to 0.12μm, both N and P MOSFETs and works for switching frequencies up to at least 3GHz.

For large-geometry transistors we generally see a significant reduction, whereas for very small-sized modern devices the noise can decrease but also increase. This is due to the very small number of traps in the transistors (sometimes only one trap) while the phenomenon depends strongly on the energy distribution of the traps. Details can be found in [4].

Other known techniques to reduce the effect of LF noise in electronic circuits are chopping and correlated double sampling. The LF noise can also be reduced by increasing gate area of the MOSFETS, at the cost of area and/or power consumption. The switched bias technique offers an orthogonal method to reduce the intrinsic LF noise in the transistor itself. It is beneficial especially in circuits where switching already occurs, such as oscillators and discrete time circuits.

Distortion Cancelling using Poly-Phase Technique

In deep submicron technology, distortion becomes an increasing problem. Large signals are required for dynamic range reasons or simply because for a given radio standard dictates the output power to be delivered by a power amplifier. The transistors, however, have less voltage gain and exhibit very non-linear behavior, which makes linear circuit design a challenge.

We know that in differential circuit the even harmonics are cancelled if the signals are in anti-phase. With this in mind, MSc student Eisse Mensink investigated whether it would be possible to use more than 2 paths and multiple phases of the signal (poly-phase) and cancel more than 2 harmonics. The basic idea is shown in **Figure 5**, where the signal path is split in N separate parallel paths.

N=2 equals the well-known differential circuit topology to cancel even harmonics. If phase shifters are available before and after the nonlinear circuit, the structure of Fig. 5 can cancel the harmonics up to N-1 [5]. The problem is however that wide-band phase shifters are very hard to implement with analog circuits. For this reason, we choose to use mixers as second phase shifters, as shown in **Figure 6**.

The mixers each have a Local Oscillator (LO) input with each a different phase, equally divided over 360/N degrees. Since we automatically get up-conversion of our input signal with these mixers, we strategically changed our plan and decided to build an RF

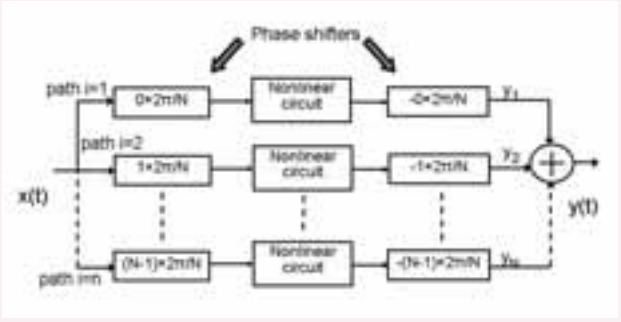

Fig. 5: N path poly-phase circuit can cancel up to the N-1th harmonic.

power up-converter. In this up-converter the first phase shifters are assumed to be implemented in the digital baseband, while in the up-conversion mixers all problematic harmonics due to nonlinearities of the N power amplifier stages can be cancelled via the poly-phase technique in combination with a 1/3 duty-cycle LO-signal [6].

A silicon realization, designed by MSc Student

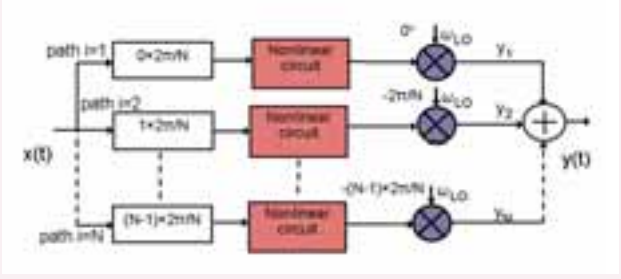

Fig 6: Wide band phase shifters can be implemented with mixers, resulting in up-converter behavior.

Rameswor Shrestha, is based on the circuit of Fig. 7 with N=18 [6]. The colors in **Figure 7** correspond to the colors of the functional blocks of Figure 6.

Rameswor demonstrated a power up-conversion mixer, which is driven in compression while all harmonics and their sidebands, up to the 17th harmonic, still remain under -40dBc. Without this poly-phase topology (i.e. for N=1) the harmonics would be below only -6dBc, which clearly demonstrates the effectiveness of the technique - 34 dB improvement. The RF frequency could be varied from DC to 2.5GHz and the final accuracy of the technique was limited by timing of the LO phases.

Conventional RF up-converters require expensive post-filters, dedicated for every RF frequency to filter out the harmonics and sidebands in order to satisfy the radio transmit mask. With this poly-phase up-converter the harmonics can be rejected and the filter demands can be much relaxed. Applications of this poly-phase up-converter can probably be found in wide band flexible up-converters and software radio transmitters, where the actual RF frequency is a priori

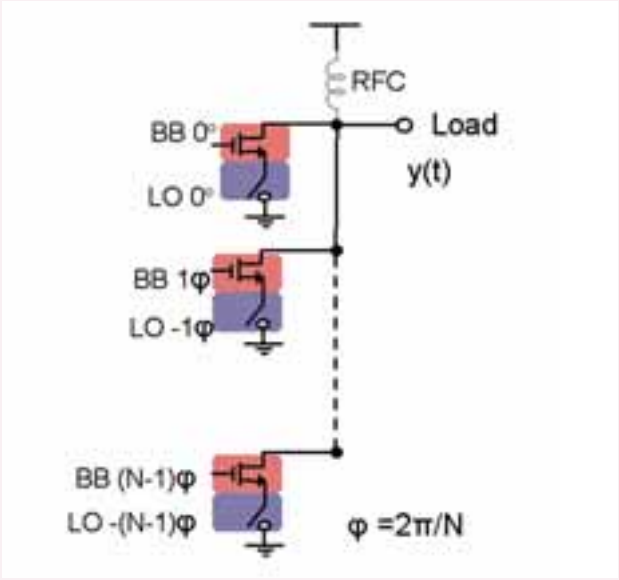

Fig 7: Basic circuit of Power up-converter.

not known and is free to be chosen in a given range.

Pulse Width Modulation Cable Equalizer

For digital data communication over copper cables, electronic equalizer circuits are used to compensate for the losses and reflections over the cables. Thanks to these electronic circuits, higher data rates can be achieved over relatively cheap cables. Examples are USB and LAN.

A well known technique used at the transmitter side is pre/de-emphasis, effectively high-pass filtering the transmitted signal. This way the low-pass characteristic of the cable is compensated for. These transmit pre-emphasis filters are generally implemented with Finite Impulse Response (FIR) filters, most often with just a few symbol spaced taps.

As an alternative to FIR filters Daniel Schinkel and Jan-Rutger Schrader proposed Pulse Width Modulation (PWM) on a digitally coded signal [7,8]: If a '1'-bit has to be transmitted, a 1-0 pattern is transmitted in one bit time and if a '0'-bit has to be transmitted a 0-1 pattern is transmitted in one bit time. This is similar to Manchester coding but with adjustable, non-50% duty-cycle. The duty-cycle of the 1-0 and 0-1 pattern is chosen in such a way that it compensates for the cable loss. This is illustrated in **Figure 8**, where the duty-cycle of a 1-0 pattern is varied and the corresponding cable responses are plotted.

Thus, by changing the duty-cycle, the transmitted spectrum, in which the lower frequencies are attenuated, is tuned for the high-frequency loss of the cable. In a real application an adaptive loop with return-channel communication takes care for this tuning, similar as in a conventional FIR approach. A test chip achieved 5Gb/s over 25m of RG-58U coaxial cable which has a loss of 33 dB at the Nyquist frequency of 2.5GHz [8] . The eye diagram for various duty-cycles is shown in **Figure 9**: for this 10m long cable 66% is the optimum duty-cycle.

The PWM technique can compensate for higher loss compensation (33 dB in contrast to approximately 20dB for 2 tap symbol-spaced FIR) because the resulting spectrum has a better match to the skin-

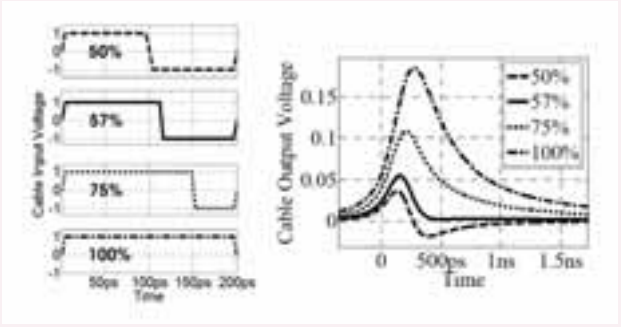

Fig. 8: Transmitting a "1" using PWM pre-emphasis: tuning the duty-cycle of the 1-0 pattern can compensate for the cable response.

effect and dielectric loss of the cable. Still only one tuning "knob" is required to fit the transfer function to the cable. Moreover the technique is insensitive to slew-rate distortion and requires only two discrete amplitudes at the TX output (with a continuously adjustable duty-cycle), which makes it suitable for modern CMOS technologies. The technique was also successfully applied earlier for very long on-chip RC limited interconnects by Daniel Schinkel and Eisse Mensink [7].

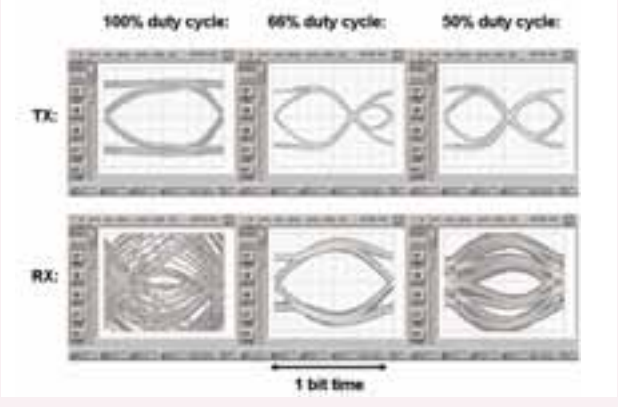

Fig 9: 5Gb/s eye patterns of transmitted signals (TX) and received signals (RX) for duty-cycle settings of 100% (normal data) , 66% (optimal PWM) and 50% (overcompensated PWM) over 10m RG-58CU cable.

Optical Detectors in Standard CMOS

Traditionally, in optical communication extremely high data rates have to be achieved over long distances. Therefore optical communication is the domain of expensive exotic technologies and the high

costs associated with it can be shared between many users. For optical communication over short distances (meters) or very short distances (optical interconnect), cost issues, however, do play a crucial role. Therefore, we started a project to integrate an optical detector in standard CMOS technology; the optical data signal can now shine directly on a digital CMOS chip. Due to the availability of low-cost high-speed laser at 850nm wavelength and the compatibility with both inexpensive plastic fibers and with photo-generation in silicon, our work mainly uses this 850nm.

An essential part of an optical detector in CMOS is the integrated photodiode structure, shown in the leftmost inset in **Figure 10**.

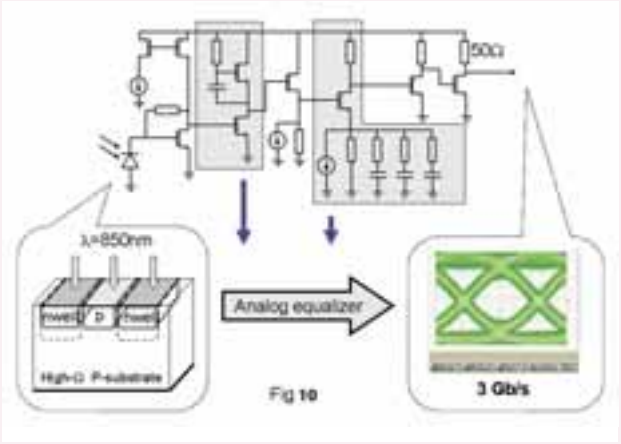

Fig. 10: Transmitting a "1" using PWM pre-emphasis: tuning the duty-cycle of the 1-0 pattern can compensate for the cable response.

Incident photons are absorbed in the silicon at tens of microns deep, much deeper than any junction in standard CMOS. In the absorption process, electrons and holes are generated and most of them slowly diffuse to the pn-junctions where the actual detection takes place. The slow diffusion causes the -3dB bandwidth of the photodiode to be in the order of 5 MHz, which causes a serious speed problem. In literature authors generally modify the technology, e.g. to allow high voltages and very wide depletion layers to boost the speed of the carriers, however this implies that non-standard CMOS has to be used. The maximal speed reported in standard CMOS so far has been 700Mbit/sec.

Ph.D. student Sasa Radovanovic implemented another solution. Although the -3dB frequency is very low, the roll-off per decade of frequency appears to be very low as well; only 3 to 4 dB per decade, up to in the low GHz region. Therefore, Sasa used an analog equalizer, with opposite frequency characteristic after the transimpedance amplifier following the diode to get a flat overall response up to a few GHz. One might assume that the production spread in time constants between the equalizer and the diode itself might ruin the performance, but thanks to the low roll off, even +/- 20% spread in time constants hardly affects the time pulses. The resulting chip achieved 3Gbit/sec in standard 0.18μm CMOS, with a BER of 10^{-11} at an optical input power of 25μW [9]. The speed limitation was in the electronic circuit, and is expected to scale with technology. This result enables high speed optical inputs for standard CMOS chips.

Conclusion

Several examples of new design methodologies have been illustrated. These methodologies benefit from modern CMOS technology and may be helpful for future system integration. More work can be found at the URL: http://icd.ewi.utwente.nl

Acknowledgements

The work described in this article has been carried out by many students; however, without the supervision or help from Eric Klumperink, Anne Johan Annema, Ed van Tuijl, Ronan van der Zee, Gerard Wienk and Henk de Vries, these results would not have been here. This work has been funded by: STW, FOM and MESA+. Philips and CERN are acknowledged for providing silicon access.

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About the Author

Bram Nauta was born in Hengelo, The Netherlands. In 1987 he received the M.Sc degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.

In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven the Netherlands, where he worked on high speed AD converters and analog key modules. In 1998 he returned to the University of Twente, as full professor heading the IC Design group, which is part of the CTIT Research Institute. His current research interest is high-speed analog CMOS circuits. Besides, he is also part-time consultant in industry and in 2001 he co-founded Chip Design Works.

His Ph.D. thesis was published as a book: Analog CMOS Filters for Very High Frequencies, (Springer, 1993) and he received the "Shell Study Tour Award" for his Ph.D. Work. From 1997-1999 he served as Associate Editor of IEEE Transactions on Circuits and Systems -II; Analog and Digital Signal Processing, and in 1998 he served as Guest Editor for IEEE Journal of Solid-State Circuits. From 2001 to 2006 he was Associate Editor for IEEE Journal of Solid-State Circuits and he is also member of the technical program committees of ISSCC, ESSCIRC, and Symposium on VLSI circuits. He is co-recipient of the ISSCC 2002 "Van Vessem Outstanding Paper Award."

Corrections continued from page 4

Fig. 4. Photomicrograph of one of the first planar integrated circuits produced by Fairchild Semiconductor in the early 1960's.

The unusual diameter of 764 microns was chosen because we were working in English units and that is thirty thousandths of an inch, or 30mils. The minimum feature size is the three mil metal line making the circular base contact. Metal-to-metal spacing is five mils to allow the 2.5mil alignment tolerance we needed.

Interestingly enough at the time the idea for the planar transistor was conceived by Jean Hoerni in the early days of Fairchild Semiconductor, it had to sit untried for a couple of years, because we did not have the technology to do four aligned mask layers. In fact, we were developing the technology to do two aligned oxide-masked diffusions plus a mesa etching step for transistors. The original step and repeat camera that Bob Noyce designed using matched 16mm movie camera lenses had only three lenses, so it could only step a three-mask set. We had to wait until the first mesa transistors were in production before we could go back and figure out how to make a four mask set to actually try the planar idea.

The first integrated circuit on the graph is one of the first planar integrated circuits produced. It included four transistors and six resistors. It has always bothered me that the picture of this important device that got preserved was of the ugly chip shown in Fig. 4. The circuit had six bonding pads around the circumference of a circle for mounting in an 8-leaded version of the old TO-5 outline transistor can. In this case only six of the eight possible connections were required. We did not think we could make eight wire bonds with reasonable yield, so for these first integrated circuits we etched a round die that let us utilize blobs of conducting epoxy to make contact to the package pins. For the die in the picture, the etching clearly got away from the etcher.

A prior version of "The Mythology of Moore's Law," by Tom R. Halfhill in the September 2006 issue was published in Microprocessor Report of December, 2004.

A 30 Year Retrospective on Dennard's MOSFET Scaling Paper

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More than three decades have passed since the team of Robert Dennard, Fritz Gaensslen, Hwa-Nien Yu, V. Leo Rideout, Ernest Bassous and Andre LeBlanc from the IBM T. J. Watson Research Center wrote the seminal paper describing MOSFET scaling rules for obtaining simultaneous improvements in transistor density, switching speed and power dissipation [1]. At the time of this paper (1974), commercially available circuits were using MOSFETs with gate lengths of approximately 5 microns, but devices with shorter gate lengths were already being built in laboratories that were demonstrating the benefits of further scaling. The scaling principles described by Dennard and his team were quickly adopted by the semiconductor industry as the roadmap for providing systematic and predictable transistor improvements.

Table I is reproduced from Dennard's paper and summarizes transistor or circuit parameter changes under ideal scaling conditions, where κ is the unitless scaling constant. The tantalizing benefits of MOSFET device scaling immediately leap out from this table: as transistors get smaller, they can switch faster and use less power. But of course learning exactly *how* to make transistors smaller in a way that could be done practically in high volume manufacturing would take time. It would take time to develop lithographic techniques to pattern smaller feature sizes, to grow thinner gate oxides, and to reduce defect levels at these increasingly challenging dimensions. But this paper gave our industry a roadmap, a method for setting targets and expectations for coming generations of process technology. This paper gave us the more specific transistor scaling formula needed to continue Moore's Law, which was first articulated in a paper by Gordon Moore in 1965 and was in effect being followed by the semiconductor industry since the early 1960's. (To read reprints of Gordon Moore's 1965 and 1975 papers along with recent commentaries on Moore's Law, see the September 2006 issue of the *IEEE Solid-State Circuits Society Newsletter.*)

The ideas described in Moore's and Dennard's papers set our industry on a course of developing new integrated circuit process technologies and products on a regular pace and providing consistent improvements in transistor density, performance and power. Each new generation of process technology was expected to reduce minimum feature size by approximately 0.7x (κ ~1.4). A 0.7x reduction in linear features size was generally considered to be a worthwhile step to take for a new process generation as it provided roughly a 2x increase in transistor density. During the 1970's and 1980's the semiconductor industry was introducing new technology generations approximately every 3 years. This translates to transistor density improvements of ~2x every 3 years, but this was also a period when average chip sizes were increasing, resulting in transistor count increases of close to 4x every 3 years (or 2x every 18 months). Starting in the mid-1990's our industry accelerated the pace of introducing new technology generations to once every 2 years and that pace continues to this day (see Figure 1). The trend of increasing chip size has slowed due to cost constraints, so we have settled into a trend of roughly doubling transistor density and transistor count every 2 years (see Figure 2).

Even more surprising, from a MOSFET scaling perspective, is that over the past 10 years MOSFET gate lengths have been scaling faster than other minimum feature sizes (see Figure 1). Prior to the mid-1990's,

Table I: Scaling Results for Circuit Performance (from Dennard)

Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	$1/\kappa$
Doping concentration *Na*	κ
Voltage *V*	$1/\kappa$
Current *I*	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time/circuit *VC/I*	$1/\kappa$
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1

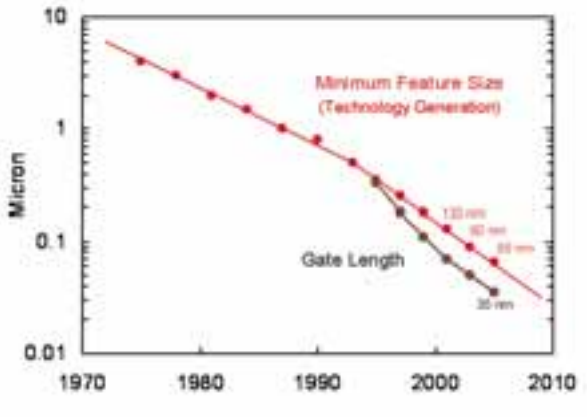

Figure 1: Feature size scaling for Intel logic technologies

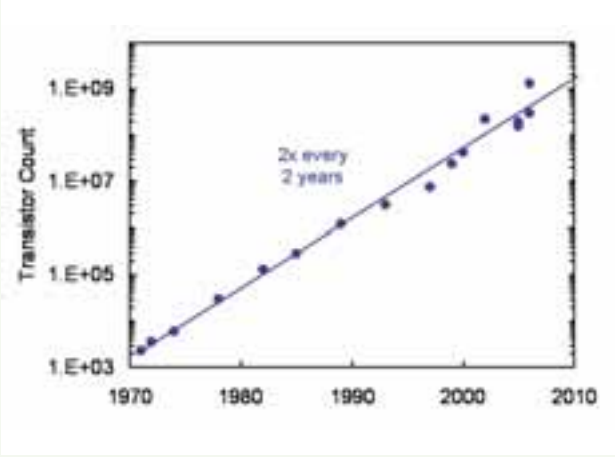

Figure 2: Transistor count trend for Intel microprocessors

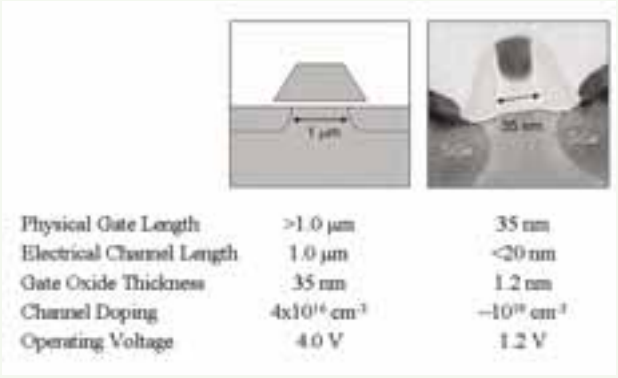

Figure 3: MOSFET structure from Dennard's 1974 paper (left) and from Intel's 65 nm generation logic technology in 2005 (right)

gate lengths were roughly the same size as other minimum process features, but starting with the 0.35 μm generation, gate lengths have been scaling faster than 0.7x per generation to realize performance advantages, even though gate pitch has been scaling at the normal rate. This has been a key factor in microprocessors achieving >3 GHz operating frequencies sooner than most experts thought possible even 10 years ago. It is exciting to see in Figure 3 how far we have taken Dennard's scaling law by comparing the 1 mm transistor described in his 1974 paper to the 35 nm gate length transistor used in Intel's 65 nm generation logic technology that started high volume manufacturing in 2005 [2]. The Intel transistor shown in Figure 3 provides an example of an emerging trend among semiconductor manufacturers: the introduction of new structures and materials to extend transistor scaling. In this case the new feature is selectively deposited SiGe source-drains to provide strained silicon for improved transistor performance [3].

Just as there have been questions about the end of Moore's Law, there have also been questions about the end of MOSFET scaling. In both cases, the answer is that the end is not yet in sight, although we face growing challenges in their continuation. Voltage scaling has been an extremely important component of MOSFET scaling because it maintains constant electric field, which is important for reliability, and it lowers transistor power, which is needed to maintain constant power density. But even in the early days of MOSFET scaling it was difficult to follow ideal voltage scaling requirements because of the need to use industry standard voltages, such as 12V, 5V, 3.3V, etc. Eventually we were able to deviate from standard voltage levels on key products such as microprocessors and were free to adjust product voltage levels to meet specific performance and power targets. More recently, however, voltage scaling has run into lower limits imposed by threshold voltage (V_T) scaling limits [4]. Dennard's scaling law assumed that V_T would scale along with operating voltage, and thus provide improved performance and power. But this 1974 work ignored the impact of transistor sub-threshold leakage on overall chip power. Sub-threshold leakage was relatively low in the 1970's and was a tiny contributor to total power consumption on logic circuits. But after 30 years of scaling, V_T has scaled to the point where sub-threshold leakage has increased from levels of $<10^{-10}$ amps/mm to $>10^{-7}$ amps/μm. Due to leakage constraints, it will be difficult to further scale V_T and thus it will also be difficult to scale operating voltage.

Another key assumption in Dennard's scaling law was the ability to scale gate oxide thickness. Gate oxide scaling has been a key contributor to scaling improvements over the past 30 years, but this trend is also slowing due to leakage constraints (see Figure 4). Intel's 65nm generation transistors use a SiO_2 gate dielectric with a thickness of 1.2 nm [2]. This dielectric is only about 5 silicon atomic layers thick and represents what is likely the limit to which SiO_2 can be scaled. Not only are we running out of atoms, but gate oxide leakage due to direct tunneling current is becoming a noticeable percentage of overall chip power.

Dennard's scaling law assumed that channel doping concentration could be continually increased to enable shorter channel lengths with the appropriate V_T. When channel doping concentration gets too high

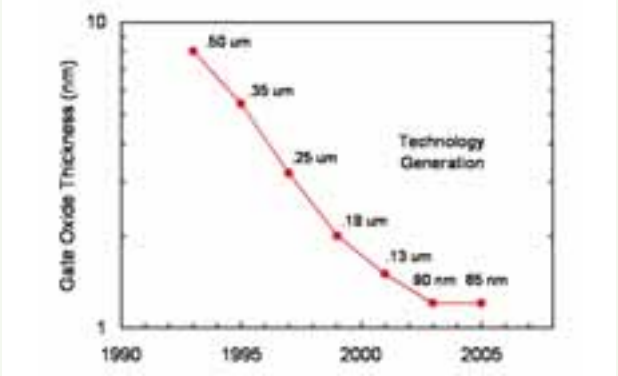

Figure 4: Gate oxide thickness trend for Intel logic technologies

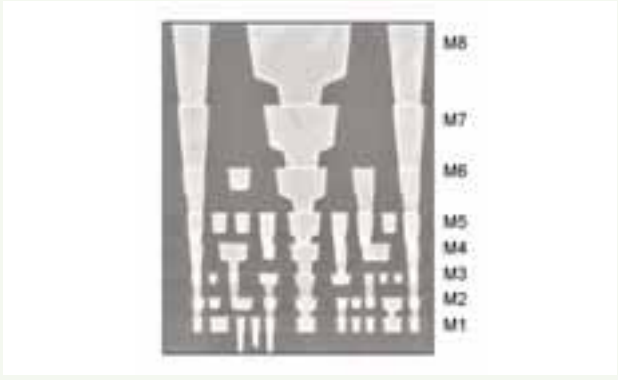

Figure 5: Copper interconnects with low-_ dielectrics from Intel's 65 nm logic technology

two problems occur: 1) carrier mobility and performance degrade due to increased impurity scattering, 2) source and drain junction leakage increases due to direct band-band tunneling. Junction leakage is already a limiter for ultra-low power integrated circuits and will eventually be a limiter for mainstream microprocessor products.

Although Dennard's paper is best known for articulating MOSFET scaling rules, less noticed was the paper's description of interconnect scaling results, as reproduced here in Table II. The key point of this table is that scaled interconnects, unlike scaled transistors, do not speed up. Scaled interconnects provide roughly constant RC delays because the reduction in line capacitance is offset by an increase in line resistance. This was not much of a concern in 1974 when interconnect delay was typically a small portion of circuit clock cycle times. But more modern logic technologies have been wrestling with the constraints imposed by interconnect delay and interconnect density [5], and have been addressing these constraints by adding more metal layers, converting from aluminum to more conductive copper wires, and replacing SiO_2 dielectrics with low-κ dielectrics to reduce capacitance (see Figure 5).

As briefly described above, scaling transistors beyond the 65 nm generation will clearly have more challenges to contend with. It is also commonly recognized that following the simple scaling rules described by Dennard and his team back in 1974 is now no longer a sufficient strategy to meet future transistor density, performance, and power requirements. But ours is a very inventive industry and new transistor technologies such as strained silicon, high-κ dielectrics, metal gates and multiple-gate devices have been or will be introduced to continue scaling. So although the letter of "Dennard's Law" can no longer be followed, it has gotten us very far over the past 30 years and the spirit is alive and well in transistor R&D facilities around the world.

Table II: Scaling Results for Interconnect Lines (from Dennard)

Parameter	Scaling Factor
Line resistance, $R_L = \rho L/Wt$	κ
Normalized voltage drop IR_L/V	κ
Line response time R_LC	1
Line current density I/A	κ

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Bohr was born in Chicago, Illinois in 1953. He received the B.S. degree in industrial engineering in 1976 and the M.S. degree in electrical engineering in 1978, both from the University of Illinois, Urbana-Champaign. In 1998 he received the Distinguished Alumnus Award from the University of Illinois department of Electrical and Computer Engineering. Bohr is a Fellow of the Institute of Electrical and Electronics Engineers and was the recipient of the 2003 IEEE Andrew S. Grove award. In 2005 he was elected to the National Academy of Engineering. He holds 42 patents in the area of integrated circuit processing and has authored or co-authored 40 published papers.

Device Scaling: The Treadmill that Fueled Three Decades of Semiconductor Industry Growth

Pallab Chatterjee, i2 Technologies, Inc.

In 1974 Robert Dennard, etal[1], wrote a paper that explored different methods of scaling MOS devices, and pointed out that if voltages were scaled with lithographic dimensions, one achieved the benefits we all now assume with scaling: faster, lower energy, and cheaper gates. The lower energy per switching event exactly matched the increased energy by having more gates and having them switch faster, so in theory the power per unit area would stay constant. This set of linear scaling principles of MOS technology has served as the treadmill on which the entire Semiconductor Industry has grown for the past three decades.

Scaling in the 70's: The Era of NMOS Dynamic Random Access Memories

The late 70's NMOS based DRAMs led the technology scaling charge in a world that was still largely bipolar and dominated by TTL logic chips. The first rounds of the application of scaling theory were focused on DRAMs. Unique clock design schemes for DRAMs devised at Mostek and technology from Intel and IBM ushered in the 16k bit VLSI DRAM, the pride of the late 70's.

Japan's MITI created the VLSI Technology Project[2], a consortium of five top Japanese microelectronics companies: Hitachi, NEC, Fujitsu, Mitsubishi and Toshiba. This consortium developed a complete technology infrastructure for the 256K DRAM and launched into the 1 micron VLSI era with strong progress in ultra clean technologies which gave Japan the lead in VLSI manufacturing in the early 80's.

The Early 80's: Crossing the Micron Barrier

Even though the scaling charge was led by NMOS, power and ease of design considerations favored CMOS Technology as the industry workhorse. The world, however, was stuck at the TTL voltage and logic level standard or 5V. The resistance to scaling voltage in the early 80's from system designers backed into the semiconductor world. This led me to propose a quasi constant voltage scaling[3].The emergence of voltage tolerant device structures like the lightly dope drain (LDD) transistor, silicide clad source drain, and hot electron defense resulted from this. These technologies provided some of the keys to continue scaling feature sizes slower than voltage and continuing the treadmill for the Semiconductor Industry.

ASIC and CAD Transforms the Chip Design Industry

Carver Meade and Lynn Conaway in their classic book, 'Introduction to VLSI Systems', used the notion of linear relationships between different device geometries to simplify the "design rules" that abstracted the manufacturing constraints from design. Linear device scaling theory also allowed simplification of a very complex interaction of process and device physics with design.

Device models to represent the complex physics of CMOS devices in circuit simulators, like SPICE, provided the abstraction between circuit theory and device physics. Based on these abstractions the industry was able to rapidly develop design tools and systems. The University of California, Berkeley[4] was a leader in developing a suite of design tools that connected logic level design to circuit design to physical design and verification tools to check for design rules. The entire ASIC world of semi-custom chips opened up based on this set of abstractions and made scaling applicable to all chips.

The Emergence of TCAD: Systematic Technology Design

The notion of creating generations of process technology that could be used for a variety of applications was emerging simultaneously with the ASIC movement to systematize chip design. Linear scaling factors began to be used as the names of the generation of technology and an informal time table started being discussed across the industry. A team at Stanford University initiated a whole new field of technology CAD[5] with Process Simulators and Device Simulators. This allowed systematic design of process and devices using formal design of experiment methods.

Manufacturing yield and defect analysis did not come under the purview of scaling theory and threatened to stop the scaling treadmill. Redundancy and repair techniques based on laser links were the initial answer to continue memory scaling beyond 256 Kbit. This was followed by yield analysis tools that were developed at Carnegie Mellon University[6]. Defect measurement tools offered by KLA, systematic yield analysis and ramp processes made the technology treadmill continue to move down the linear scaling path.

Single Wafer Manufacturing Systems for Scaling to Larger Wafers with Sub Half Micron Features

From 1988 through 1993 Texas Instruments partnered with DARPA, the U.S. Air Force, semiconductor equipment makers, and university researchers in the Microelectronics Manufacturing Science and Technology (MMST) Program[7]. Its purpose was to develop advanced IC manufacturing technologies enabling dramatic

improvements in process control, cycle-time, and overall flexibility and continue the scaling of devices to deep submicron to cost effectively. In particular, the MMST Program demonstrated the technical feasibility of 100% single-wafer processing, dynamic/object-oriented Computer-Integrated-Manufacturing (CIM), real-time/model-based process control, in-situ sensors, 95% dry processing, and integrated mini environments.

At that time, state-of-the-art commercial wafer fabs used a mix of approximately 60% single-wafer and 40% batch processing equipment. Since then, complete sets of commercial single-wafer process tools have become available and are the norm for deep submicron manufacturing.

The most significant contribution of MMST to single-wafer processing was in the area of Rapid Thermal Processing (RTP). In contrast to large furnaces for thermal processing, the MMST program developed processing chambers in which single wafers were heated by lamps under multi-zone, closed-loop wafer-temperature control. Some of the initial MMST work on RTP lamps was performed in collaboration with Stanford University. Applied Materials, Inc. subsequently introduced RTP on their Centura HT™ cluster tool. MMST also created the first lithography cluster tool and the concept of the vacuum carrier which is more popularly knows as the SMIF box.

SIA Industry Roadmap

In November 1992, 179 of the key semiconductor technologists of the US gathered in Irving, Texas for a historic workshop to create a common vision for the course of the semiconductor industry for the next 15 years based on scaling technology[8]. The group consisted primarily of scientists and engineers from the US Semiconductor Industry and a liberal sprinkling of academics, government agencies and national laboratories. The workshop, sponsored by the Semiconductor Industry Association and coordinated by Semiconductor Research Corporation and Sematech, created the roadmap below.

1992 SIA Overall Roadmap Technology Characteristics

	1992	1995	1998	2001	2004	2007
Feature Size (μm)	0.5	0.35	0.25	0.18	0.12	0.10
Gates/chip	300k	500k	2M	5M	10M	20M
Bits/Chip - DRAM - SRAM	16M 4M	64M 6M	256M 64M	1G 256M	4G 1G	16G 4G
Wafer processing cost ($/cm2)	$4.00	$.390	$3.80	$3.70	$3.60	$3.50
Chip Size (mm2) -logic processor -DRAM	250 132	400 200	600 220	800 500	1000 700	1250 1000
Wafer Diameter (mm)	200	200	200-400	200-400	200-400	200-400
Defect Density (Defects per cm2)	0.1	0.05	0.03	0.01	0.004	0.002
No. of interconnect levels - logic	3	4-5	5	5-6	6	6-7
Maximum Power (watts per die) -high performance -portable	10 3	15 4	30 4	40 4	40-120 4	40-200 4
Power supply Voltage (V) -desktop -portable	5 3.3	3.3 2.2	2.2 2.2	2.2 1.5	1.5 1.5	1.5 1.5
No. of I/O's	500	750	1500	2000	3500	5000
Performance (MHz) -off chip -on chip	60 120	100 200	175 350	250 500	350 700	500 1000

Five areas of critical challenges that could decrease the rate or even stop the progress of scaling of Semiconductor technology were identified:

- Patterning material and processes for device structures below 0.25μm
- Electrical interconnections, both on and off chip
- Electrical test, time cost and capability
- Design, modeling, simulation capability for all elements of IC technology and products
- Software capability, availability and quality for all aspects of IC technology and production.

As we look back at the last 15 years now at the end of 2006, this roadmap has truly focused the investment and made most of the predictions come true.

Emergence of Foundry Manufacturing Companies

As the process technology scaling became more systematic the disaggregating of IC manufacturing became a reality. Since the establishment of TSMC in 1987 to satisfy customers' needs under the disintegration trend, the pure play foundry industry has grown to a multi-billion business. In turn, the pure play foundry business model has further accelerated the disintegration trend in the semiconductor industry.

In the past decade, leading foundry companies have caught up with the leading IDMs (Integrated Device Manufacturers) in process technology prowess. The technological challenges of foundry companies in the next decade will be even more challenging than those of leading IDMs because of the need to emphasize more on process versatility, cost effectiveness and easy adoption by diversified customers.

The specific technology development challenges of a successful foundry company in the next decade include: (1) aggressive scaling of transistors, interconnect, and design rules for both performance and density; (2) embedded technologies for SOC solutions; (3) cost effective and manufacturability process technology; (4) a versatile technology portfolio; and (5) easy integration among customers, design service/IP providers and the foundries.

In the next decade, the foundry paradigm is expected to play an even more important role as foundry companies continue to build their core competencies, including leading-edge process technologies, advanced and flexible manufacturing capabilities, and customer-oriented services systems. The strong entrenchment of the foundry industry will further move the semiconductor industry in the direction of complete disintegration.

Scaling continues to be the Treadmill of the Semiconductor Industry

Looking back at the last few years since the first SIA workshop, the ability to marshal and focus the investments of the entire industry on the key technology issues has indeed been an enabler for scaling down to 90nm. The top three among these are:

1. Sub-wavelength optical lithography (including OPC/Resolution Enhancement Techniques):

   Advances in scanners and resist technology enabled printing features less than one-half of the light wavelengths. Chemically amplified resists, light polarization, phase shifting techniques (alternating apertures and attenuated), as well as comprehensive Model Based Optical Proximity Corrections of critical layer layouts, are the key enablers.

2. Extending bulk CMOS by several performance boosters - stress/strain, ultra shallow junctions, and ox nitrides:

   Conventional bulk CMOS device architectures have been extended to 90 nm and below technology nodes by employing several performance boosters such as:
   - bi-directional stress/strain layers to enhance carrier mobility for both electrons and holes,
   - ultra-shallow junctions obtained by very low energy implants and flash/laser anneal
   - very thin (1.2 nm) gate ox nitride layers that provide uniform layers, good interface to both substrate and polysilicon gate and prevent Boron penetration.

3. Multilevel Cu interconnect including CMP:

   Up to 12 layer of Cu interconnect layers have been achieved thanks to Double Damascene Cu deposition/patterning technology and improvement in chemical mechanical polishing. Dishing/erosion effects have been reduced by applying smart dummy fill and additional manufacturability layout design rules to eliminate wide lines/small spacing patterns and drastic density variations within each interconnect layer.

As we look forward to the continuation of these 30 years of scaling progress, there are similar challenges to overcome to scale to 45nm and below:

1. Device/process variability[9]:

   Process variability sources can be categorized based on the spatial hierarchy: lot-to-lot, wafer-to-wafer, within-wafer or within-die, or root causes (random or systematic). These sources create a complicated distribution of parameters that must be addressed

by circuit designers. One of the key parameters is poly linewidth, since it has the dominant effect on MOS transistor electrical performance. For 90nm technologies, more than 50% of the variance in poly line width comes from within-die (within field) variations. The next component is die-to-die. The percentage of systematic variations increases with device scaling. For 90nm NMOS transistors, it reaches 40% of the overall Across Chip Variance (ACV).

Transistors behave differently based upon the neighborhood layout pattern due to printability and stress/strain effects. Moreover, printability and Chemical Mechanical Polishing (CMP) cause significant variations in interconnect parameters such as resistance and capacitance.

2. New device architecture (UTB, dual gates) less dependent on channel doping fluctuations:

   Despite quite a few novel device architectures proposed in recent years (FinFET, Ultra Thin Body Transistor, Inverted T FET), the bulk CMOS device architecture is used virtually exclusively at 45 nm. It will most likely dominate the 32 nm nodes, although SOI substrates are gaining more acceptance. This leaves the device performance variations very susceptible to random dopant fluctuations. Performance boosters are additive and help, but also create additional variability sources which forces circuit designers to accept much higher variability and as well as leakage currents.

3. Material improvements: high-k for gate dielectrics, porous low-k for interconnects:

   Several candidates for high-k materials have been explored; but although Hf or Zr based oxides/silicates provide attractive dielectric constant values and are stable, they do require interfacial SiO_2 layers between high-k layers and substrate/polysilicon. The final stack is not as beneficial anymore. Hence, high-k gate dielectrics are not employed in the vast majority of 45 nm technologies and only in combination with metal gates do they have a chance at 32 nm.

4. Advanced process control (especially feed forward):

   Given the increasing complexity and small process windows, yield variability is a very significant problem. Baseline process variability keeps on increasing (tails of wafer yield distributions) and the present metrology/inspection static sampling plans fail at detecting excursions in-line. New approaches for yield relevant SOC and APC are needed to take advantage of the increased process observables due to in-situ equipment sensor/FDC deployment.

5. Compact device models:

   Below 100 nm, compact device models must accommodate microscopic (i.e., "non-bulk") physical effects with minimal impact on overall computational complexities. BSIM has filled this role for many technology generations as the workhorse, both for model characterization and node-to-node technology predictions. It continues to have the confidence of industry and seems likely to remain in service (with the possible exception of RF) down to about 45 nm.

   More recent MOS models are formulated as functions of surface potential, rather than threshold voltage, in the channel and s/d edges. Surface potential is directly linked to intrinsic channel charge dynamics and enables addition of important physical effects with an economy of model complexity. The formulation admits an expression for transistor drive current that is continuous from accumulation to saturation, thereby avoiding the necessity of matching multiple regions.

Compact models at 65 nm have high priority needs for improvement:

(a) scalability of sub-threshold currents and output resistance from short-to-long channel lengths, due largely to lateral doping non-uniformities
(b) dependence of noise on voltage and geometry; i.e., considering 1/f noise dependence on random noise trap occurrences
(c) capabilities for handling geometrical statistical fluctuations which affect noise, threshold voltage and drive current.

The above problems become more severe at 45 nm, along with the following additional priorities:

(1) gate current scaling and dependences on novel (e.g., multi-layer) gate stacks,
(2) carrier mobility in the channel due to layout-induced stress/strain,
(3) statistical variations stemming from random dopant placements,
(4) ballistic transport of carriers in intrinsic channel and,
(5) quantum mechanical effects due to confinement in thin films.

Summary

Scaling theory has been the organizing principle of the progress of the semiconductor industry throughout three decades. It has created a framework for continued improvement in density and cost performance and facilitated the desegregation of the entire industry

around design and manufacturing. Few concepts in our time have had as much influence on the economy.

Acknowledgement

I would like to thank Ping Yang, Bob Doering, Andrzej Strojwas, Robert Dutton, Bill George, Lawrence Arledge, and Alberto Sangiovanni-Vincentelli for providing perspectives on the various aspects of impact of scaling on the semiconductor industry for this paper.

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Chatterjee worked at Texas Instruments from 1976-2000. During his tenure there he held various executive positions. Under his leadership as senior vice president of Research and Development and chief technology officer, the Texas Instruments Technology Labs became known as a standard for excellence acknowledged by both academia and industry. As TI's senior vice president and chairman of the Manufacturing Excellence team, he was responsible for manufacturing improvements which delivered hundreds of millions of dollars in bottom-line improvement. As president of TI's Personal Productivity Products (calculators and PC business), he contributed to increasing Texas Instruments' market share and managed more than $1.5 billion worldwide. In the role of chief information officer, he led the global i2 and SAP implementation and process transformation for Texas Instruments.

During Chatterjee's tenure at Texas Instruments, he was a TI senior fellow in 1985, an IEEE fellow in 1986, and received the IEEE J. J. Ebers award in 1986. He was elected a member of the National Academy of Engineers in 1997.

Chatterjee has been awarded numerous patents and has written several publications on the high technology industry. He earned a Bachelor of Technology degree in electronics and communication engineering from the Indian Institute of Technology, Kharagpur, India. As a student there, he was awarded the President of India Gold Medal as the class valedictorian and the B.C. Roy Memorial Gold Medal for extracurricular excellence. He received his master's and doctorate degrees in electrical engineering from the University of Illinois, and was awarded a honorary Doctor of Science Degree from Indian Institute of Technology, Kharagpur, India.

Recollections on MOSFET Scaling

By Dale L. Critchlow, IBM Fellow, Retired; Dale.Critchlow@uvm.edu

The Beginnings

By 1970 the MOSFET technology was finding its way into manufacturing in a number of companies.[1] Bob Dennard and I were part of the team that developed the NMOS technology (2) in the T. J. Watson IBM Research Laboratories in the 1960s. The first IBM NMOS MOSFET product, which was entering large scale manufacturing, was a high-speed main-memory with a 50ns typical access time (100ns spec) at the board level. It used 1Kb chips (soon replaced with 2Kb chips) with a six-device cell using off-chip bipolar sense amplifiers and high level decoders proposed by Peter Pleshko and Lewis Terman (3). These chips replaced the bipolar main-memory technology which had been introduced a couple of years earlier to replace ferrite core memory.

In mid-1970, IBM Research management was searching for a technology to fill the "file gap" between moveable head magnetic disks and random access main-memory for transaction based systems. This performance gap was being filled by expensive fixed head HDDs which had much smaller latency time than the moveable head HDDs. Don Rosenheim (Manager of Applied Research) and Sol Triebwasser challenged my department to develop a proposal for a "monolithic file" with a cost/bit of about 1 millicent/bit or 1/1000 of the projected main-memory cost. Bob Dennard was manager of a small group including Fritz Gaensslen and Larry Kuhn which reported to me. There were a number of options including shift registers and CCDs, but Dennard as the inventor was keen on pursing the one-transistor DRAM cell. Bob did some preliminary analyses, and concluded that we would need feature sizes of about 1μm, a 5X shrink from those in manufacturing, to achieve our goals.

We realized that we would have to scale the vertical dimensions (oxide thickness and junction depth) and adjust the doping level of the substrate to maintain usable device characteristics. Further, we would have to scale the operating voltages as well to preserve reliability and limit power dissipation. In fact, we had done this twice before in the 1960s, first from 24V to 12V and then to 6V using rudimentary scaling to guide our designs. (Engineers of that era, before the advent of computer simulation, were well versed in design by similitude or scaling.) We observed that our current transistors with channel lengths of 5μm and gate oxide thickness of 100nm could be operated at 20V. Therefore, we could scale to a 4V power supply with a 1um, 20nm transistor. We noted that the circuits would consume less power and be faster. Within a few days Bob, Fritz and Larry had formalized the constant-field scaling theory and its limitations.

The implications of scaling were remarkable. If all dimensions, voltages (including threshold voltage) and doping levels were scaled by a constant factor κ: a) the circuit delay was decreased by κ, b) the power/circuit was decreased by κ^2, and c) the power delay product was reduced by κ^3. Further, the power/unit area of silicon remained constant! These were exactly the results we needed to develop a competitive low cost memory. On the down side, there were questions about the scalability of the threshold voltage and the fact that the IR drops and RC time constants of the interconnects become more severe with scaling. Of course, there were a host of transistor design, process and reliability challenges.

At that point, we were convinced that MOSFET memory would replace fixed head files. Further, we speculated that it may also replace moveable head disk storage for some applications. We also started to believe that the MOSFET would someday replace the bipolar transistor in high-performance logic and memory applications.

Driving the Demonstration and Implementation of Scaling was Key

Bob Dennard's most profound contributions were to demonstrating the feasibility of MOSFET scaling, and then leading the way into implementation in real products. He worked with a succession of very talented engineers over several decades, providing guidance as well as continuing to make significant technical contributions.

The principles of scaling were first presented at the 1972 IEDM (4) along with the design and experimental characteristics of an ion-implanted 1μm transistor with a 20nm gate oxide[2] which had been optimized for scaling. One of the original slides used to describe scaling is shown in Fig. 1. (Bob remembers a high degree of skepticism about the feasibility of 20nm

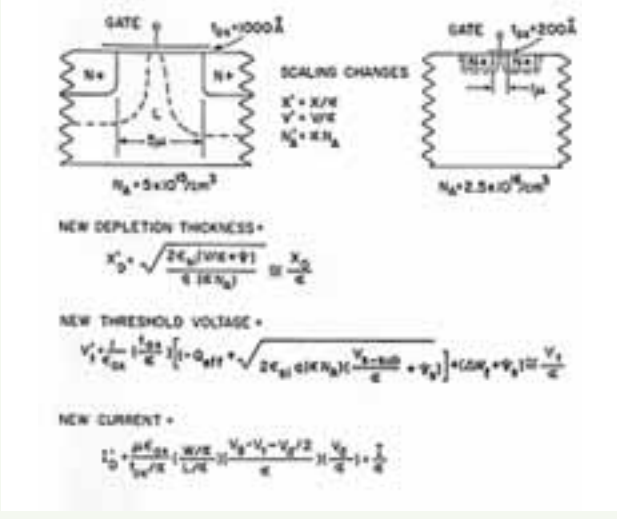

Fig. 1 Slide from 1972 IEDM showing some of the scaling principles.

oxides from the audience many of whom were struggling with making reliable 100nm oxides.) This was soon followed with a 1973 IEDM paper (6) utilizing ion-implantation to allow improved scaled transistors. The paper normally considered the "scaling paper" was published in 1974 (7). In 1975 Dennard, with others, proceeded to demonstrate scaling on a complex chip by scaling an existing 8Kb PMOS chip (originally designed in 3.75μm ground rules) by 3X and fabricating it with 1.25μm feature sizes using electron beam lithography (8). A photo of several cells and support circuits is shown in Fig. 2. Hwa Yu developed an anisotropic dry etching process which made it possible to delineate the 1.25μm features. The success of this experiment had a major impact on how seriously people took scaling both inside and outside IBM.

Attention was then turned to high-speed logic and SRAM. One of our goals was to lay the groundwork for replacing bipolar transistors in mainframe computers. This culminated in a series of eight papers (9) describing a 1μm technology that took advantage of the scaling principles. Bob was coauthor of several of the papers.

Bob continued to push the envelope with a large number of publications in cooperation with a succession of young researchers. Describing these papers is well beyond the scope of this paper. However, a few key papers stand out. In 1984, with Giorgio Baccarani and Matt Wordeman, he generalized the scaling theory to take into account the parameters which did not scale well (10). In 1985, he co-authored a definitive paper on 1μm CMOS (11) with Yuan Taur and others. In 1995, a paper laying the groundwork for a 0.1mm CMOS on SOI technology was published by Ghavam Shahidi and others (12).

In addition, Dennard furthered the cause and presented the challenges of MOSFET scaling to technical audiences outside the IEEE organization. For example, he published a paper in 1981 in the Journal of Vacuum Science and Technology (13) which showed the practicality of scaling to submicron devices and described the hierarchical wiring system needed to take advantage of scaling. In 1985 he published an authoritative paper on scaling to deep sub-micron dimensions in Physica (14).

Although he was not listed as an author, Bob had a major influence on the keystone 1988 paper (15) by Bijan Davari, et al, which described the 2.5V, 0.25μm CMOS technology which was key to the replacement of bipolar technologies for high-speed main-frame computers and microprocessors.

Technical Challenges and Advances to Make Scaling Feasible

Even though the principles of scaling, and the understanding that the MOSFET could be scaled existed in the early 1970s, the benefits of scaling could not have been accomplished without many other technical advances in the industry over the decades. There were remarkable improvements in optical lithography, dry etching, ion implantation, insulators, polycide and silicided contacts, multilevel metal, planarized BEOL, copper wiring, shallow trench isolation, packaging, design techniques, testing and characterization, design tools and system architecture. The switch to CMOS was critical to containing the level of chip power.

These improvements allowed scaling of the MOSFET technology to meet the expectations of the industry following the trends popularized in recent decades as Moore's Law (16).

The Long Delay before Switching to Lower Power Supply Voltages

While the advantages of scaling were apparent to many people, it was two decades before the power supply was scaled for mainstream products, Fig. 3. The indus-

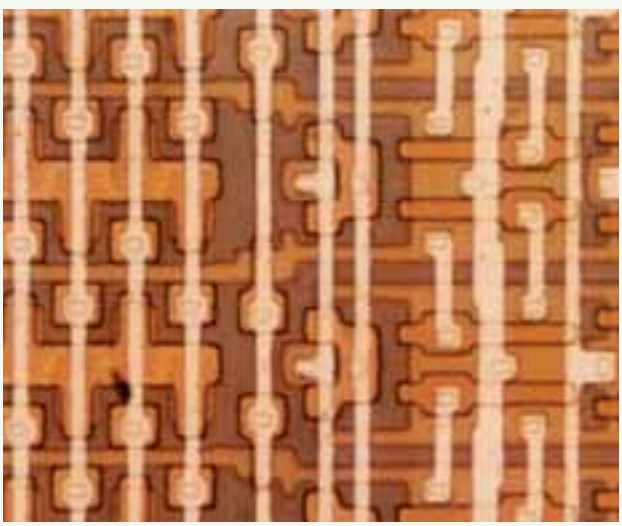

Fig. 2 Photograph of portion of experimental 8Kb DRAM chip using 1.25μm features which was scaled from a 3.75μm design.

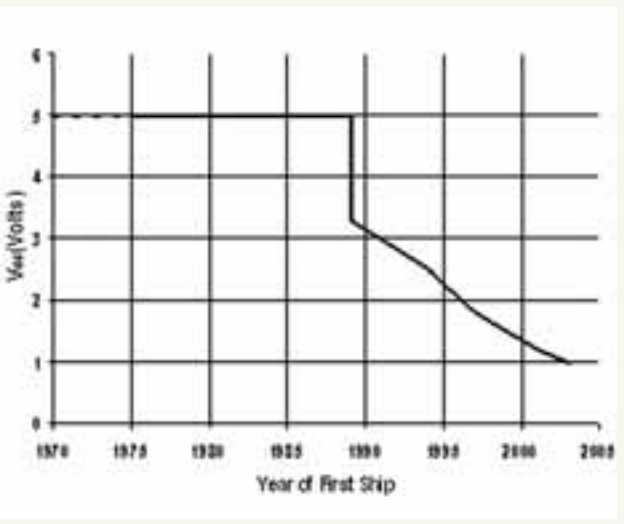

Fig. 3 Transition of mainstream MOSFET products from 5V to scaled voltages occurred two decades after scaling principles were defined.

try settled on 5V supplies in the early 1970s to be compatible with bipolar TTL. In fact, this was a lower voltage than what could have been possible for the dimensions being used. Consequently, the improvements in transistor design and chip fabrication were applied to 5V technologies, significantly improving component packing density and performance over several generations. Further, the LDD device (17) allowed reliable operation and high performance at 5V. The tighter tolerances necessary to make scaling practical improved 5V designs as well, reducing the performance advantage of full scaling. Most importantly, the whole computer industry was optimized around a 5V power supply and very successful products were being delivered. An earlier switch to a lower voltage would have been greatly disruptive to the designers, the manufacturers and in the marketplace.

The 5V standard finally collapsed in the late 1980s due to three major forces:

1) The power dissipation at 5V became untenable, especially as the circuits were driven to higher speeds.
2) The portable, battery-powered applications were demanding higher performance, low power and compatibility with battery voltages.
3) The inherent speed advantages of scaled transistors, as tolerances improved, were needed for high-speed applications.

Once the dam broke there was tremendous change within a few years, first to 3.3V then to 2.5V, etc.

The Impact of MOSFET Scaling has been Monumental

Scaled CMOS has become the dominant technology for digital and many analog applications and will continue to be a fundamental driving force of the industry for years to come.

By the late 1980s, DRAM had long displaced fixed head files in the file gap. In recent years, we have been seeing flash memory replacing disk drives in many portable applications.

The 2.5V CMOS technology (15) was the death knell for high performance silicon bipolar technologies in high-end computers. BiCMOS had gathered some momentum, but when designers came to realize that very effective off-chip drivers could be made using MOSFET circuits, BiCMOS soon faded. By the early 1990s, the high-end computers were being designed using low-voltage scaled CMOS (18) replacing bipolar chips. Bipolar and BiCMOS have found new applications for very high-speed applications using more exotic technologies.

Acknowledgements

The author is indebted to B. Davari, R. H. Dennard, E. J. Nowak and L. M. Terman for providing information for this paper. He also wishes to acknowledge a large number of outstanding engineers in IBM, other companies and Universities who shared an incredible 40 year journey in MOSFET technology.

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About the Author

Dale Critchlow is a retired electrical engineer with 35 years experience at IBM and 15 years in academia. He received his Ph.D. in Electrical Engineering from Carnegie Institute of Technology in 1956. After teaching at CIT for two years, he joined IBM Research. He became one the early members of the NMOS MOSFET project in the T. J. Watson Research Center in 1964, where he managed the MOSFET device and circuit design work through 1976. Next he transferred to the IBM Components Division, first in East Fishkill, NY, and then in Essex Junction, VT where he managed a group responsible for the advanced development of MOSFET logic and memory technologies. He retired from IBM in 1993 and was faculty member at the University of Vermont until 2005. He has active in IEEE activities and has published a number of papers and patents.

Dr. Critchlow is a Life Fellow of the Institute of Electrical and Electronic Engineers, an IBM Fellow and a member of the National Academy of Engineers.

[1] Ross Bassett wrote an excellent Ph.D. thesis and published a book [1] on the early history of the MOSFET technology. The appendices have a wealth of authoritative historical information.

[2] Concurrently, B. Hoeneisen and C. Mead published a theoretical paper [5] projecting that a 0.4mm transistor with 14nm oxides and 2V operation could be built.

The Business of Scaling

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In addition to technical challenges, managing the economics of scaling and increasing demand have been key factors in driving the semiconductor industry to nearly $250B over the last 40+ years. The functionality per chip has increased 2x every two years[1,2]. Although the cost of wafer fabs and manufacturing has increased significantly over the years, the semiconductor industry has maintained a reduction of about 29%/year in the cost per function (CPF)[3]. This translates to a halving of the CPF every two years[1]. In this paper we will provide an overview of salient business aspects and economics of scaling.

1. Introduction

Since the introduction of the first commercial integrated circuit in 1961 and the introduction of the first microprocessor in 1971, the semiconductor industry has experienced a healthy growth of approximately 15% CAGR[4]. In the mean time semiconductor sales have grown more rapidly than the worldwide electronics sales and the worldwide GDP and are now roughly 20% of worldwide electronics sales and about 2% of the worldwide GDP[4]. Fueling the growth has been increasing demand for components for personal computers, automotive, mobile wireless and consumer

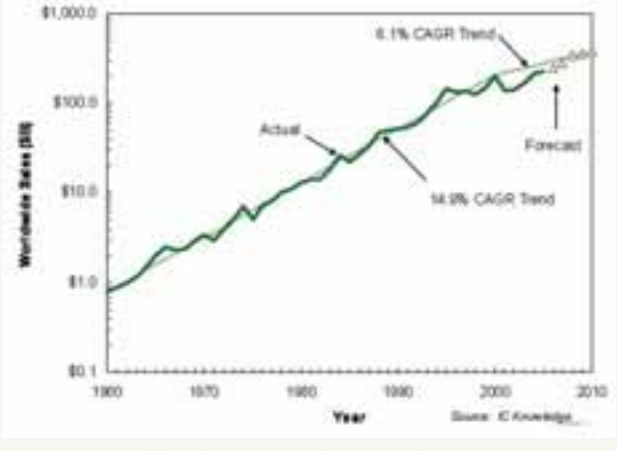

Figure 1 Worldwide semiconductor sales

products. Although the growth rate is predicted to slow down, the industry has demonstrated much resilience in combating technical and business challenges.

Taking advantage of scaling, the industry has increased the number of components per chip steadily, as shown in Figure 2. This figure shows the historical increase in the number of transistors per chip (39% per year average) in industry leading microprocessors[4]. This trend shows a doubling of the transistors per chip every two years. This trend was predicted by Gordon Moore and has become known as "Moore's Law"[1,2]. The figure also shows the reduction of minimum feature size at an average rate of 12% per year. The number of transistors per chip has increased 6 orders of magnitude while the minimum feature size has been scaled down over two orders of magnitude during the last 35 years.

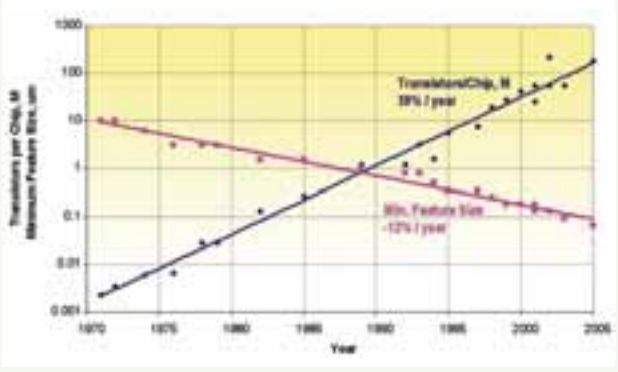

Figure 2 Historical trends of transistors per chip and minimum feature size

2. The Basic Cost Equations

The basic equation for predicting the cost of an integrated circuit die (or "chip") is:

Die Cost = Wafer Cost / Net Die per Wafer

where wafer cost is determined by factors such as facilities and equipment depreciation, materials, labor and processing cost, and

Net Die per Wafer ("NDPW") = Yield* Gross Die per Wafer ("GDPW")

Gross Die per Wafer ("GDPW") = Total usable Area on the Wafer / Die Area

Yield is a function of defectivity (or defect density) and critical area. Contributors to defectivity are usually categorized as systematic (or gross) and random defects[3]. Many different yield models have been used in the industry. Simple models, such as the Poisson and the Murphy models using the die area as the critical area were prevalent in the early days. The Bose-Einstein model using die area but identifying a defectivity per critical layer has been used extensively in recent years[8,9]. Custom models exist at captive suppliers. More recently, sophisticated calculations of critical area based on information embedded in the design database are being used to estimate yield. Examples are the number of vias and contacts in a design, the number of metal layer cross-overs, and the like. A detailed discussion of these is beyond the scope of this paper.

3. Overall Cost Reduction

A key factor in managing the business feasibility of scaling is the semiconductor industry's ability to maintain an overall CPF reduction of 29%/year[3] to 35%/year[4]. Within any given process technology node the die cost and CPF are reduced due to the manufacturing and defectivity learning curves. This is shown graphically in a conceptual chart, Figure 3. As the volume of wafer and product shipments ramps up in each technology node, there is a reduction in die cost (and therefore CPF) due to a reduction in wafer cost; this decrease is due to process optimization and the manufacturing learning curve. Also, die cost is reduced as yield enhancement efforts are implemented, defectivity is reduced, yield increases and therefore NDPW increases. A compilation of defect density trends indicates an average reduction of 19% per year over the last 35 years[4]. The technology "cross-over" occurs when the CPF in the newer technology is below the CPF in the older technology.

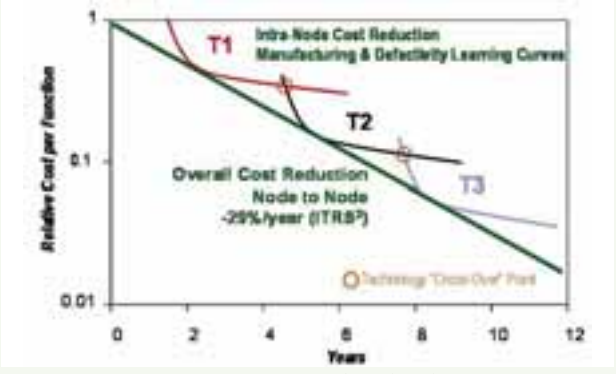

Figure 3 Cost per function and technology "cross-over" points

4. Cost Reduction from Technology Scaling

An industry target has been to reduce minimum feature size by around 30% at every process technology transition. Table 1 shows the various process technology generations or "technology nodes" used since the mid 1980's.

Table 1 Scaling ratio for various technology nodes since the mid 1980's

Technology Node, um	Scale Factor, k
1.5	
1	0.67
0.8	0.80
0.6	0.75
0.5	0.83
0.35	0.70
0.25	0.71
0.18	0.72
0.13	0.72
0.09	0.69
0.065	0.72
0.045	0.69
0.032	0.71

Such technology scaling was achieved typically in the following manner:

a. Drive new photo lithography equipment and processes that allowed printing and patterning of dimensions 30% smaller than in the previous generation.
b. Make improvements to other parts of the process, e.g., gate oxidation, ion implantation, diffusion, etching, interconnect metallurgy etc.
c. Engineer and optimize the transistor device structure and various aspects of the process to meet performance and cost goals, and be manufacturable and reliable.
d. Execute a "**Linear Shrink**" of an existing product reducing the die size by a scaling factor such as 0.7. Due to various intricacies of the process, the design rules and device characteristics at shrinking geometries, such scaling became increasingly difficult. In the mid-1980's such an approach, which was referred to by some people as a "dumb shrink" became known as an "intelligent laborious shrink" at some companies.
e. A new set of design rules - both physical and electrical - were usually used to design new products that took full advantage of the new technology capability. While the shrink approach was able to get an initial product out in the new technology node, the "**Re-Design**" approach was necessary to maximize performance and minimize cost of products in the new node.
f. In addition, the new technology usually had some new features aimed at increasing the packing efficiency, design productivity and device performance. Some examples are: increasing the number of metal interconnect layers, self-aligned polysilicon gate structure, oxide and trench isolation, standard cells, EDA tools and re-usable IP blocks.

We will now discuss migration of designs from one node to the next using either the "**Linear Shrink**" or the "**Re-Design**" approach. To illustrate the "**Linear Shrink**", consider Figure 4(a), which depicts a square die with dimension y and having N transistors, in technology node T1. A simple shrink of the die into technology node T2 would reduce the die size by the scale factor k, where 0<k<1. It should be noted that this scaling factor corresponds to the factor $1/\alpha$ used by Dennard in his papers[5]. Table 2(a) is a summary of the resulting scaling parameters as well as typical values for such a scaling. Although the cost to process the wafer in the new technology node increases by a factor C (typically a 20% premium), the die cost and the CPF reduces to Ck^2 or 60% of the cost in the technology node T1, for k=0.7. This initial analysis assumes the new technology is processed using the same wafer size, and that the yield is the same in both technologies.

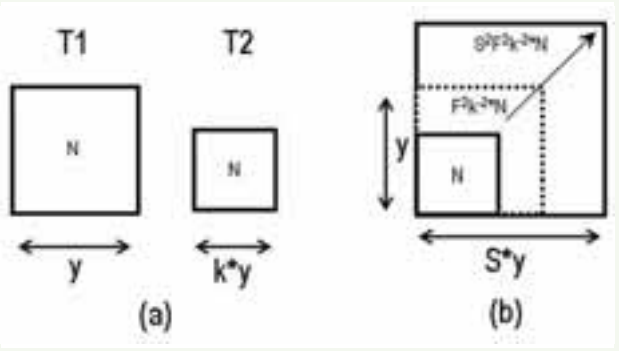

Figure 4 (a) "Linear Shrink" from technology T1 to T2 and (b) "Re-design"

(a) LINEAR SHRINK Constant Wafer Size Constant Yield	T1	T2	Typical
Technology Scale Factor	1	k	0.7
Die Size	1	k	0.7
Wafer Cost	1	C	1.2
GDPW	1	k^{-2}	2
Die Cost	1	Ck^2	0.6
# Functions	1	1	1
CPF	1	Ck^2	0.6

Table 2 (a) Summary of scale factors for a "Linear Shrink"

The "Re-Design" approach is illustrated via Figure 4(b) which depicts increased packing density achieved by taking advantage of more aggressive technology features and design rules and a "Cleverness Factor", F. The number of transistors packed in the same size die increases by a factor F^2k^{-2}. Further increases in packing density resulted from the use of larger die sizes. Manufacturing enhancements of the process, the equipment and the clean room environment resulted in lower defect densities. This allowed the fabrication of larger dice with acceptable yields in the new technology node in spite of the tighter geometries. The increase in the maximum allowed die size is represented by the factor S. For simplicity, we assume a square die and "die size" represents one linear edge of the die. Table 2(b) summarizes the scale factors and typical values. These typical values show a 29% annual reduction in CPF, a 4x increase in functions over a 3 year period, which is consistent with Moore's Law[1, 2] and the ITRS 2005[3].

(b) RE-DESIGN including Increased Die Size and New Technology Cleverness Constant Wafer Size Constant Yield Increase Die Size to Increase Packing Density	T1	T2	Typical
Technology Scale Factor	1	k	0.7
Die Size	1	S	1.1
Wafer Cost	1	C	1.2
GDPW	1	S^{-2}	0.9
Die Cost	1	CS^2	1.4
Cleverness Factor	1	F	1.3
# Functions	1	$S^2F^2k^{-2}$	4
CPF	1	$CF^{-2}k^2$	0.36
CPF reduction/year, 3yr cycle			29%

Table 2 (b) Summary of scale factors for "Re-Design"

Such a scaling methodology has been reported by Intel for their 80x86 microprocessors. Figure 5 shows the migration of the 8086, 80286 and the 80486

processors with increasing transistors per chip[6]. For example, in 1989 the 8086 and 80286 microprocessors fit into an area that was a fraction of the area in previous technology generations. Then the 80486 was introduced in the new node with a larger die size and 4x the number of transistors of the previous processor in the previous node.

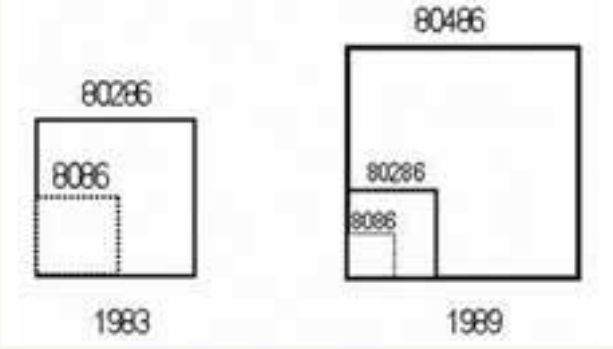

Figure 5 Technology scaling methodology reported by Intel

5. Die Cost Reduction by Increasing Wafer Size

The industry has successfully increased wafer size[7] from 50mm (2") to 300mm (12") as shown in Figure 6. The wafer diameter steps result in either a 1.33x or a 1.5x diameter ratio versus the previous size. An increased number of gross die per wafer results from the use of larger diameter wafers, as shown in Figure 7. The available silicon area is either 1.78x or 2.25x for the two different diameter ratios. The actual ratio of GDPW is generally higher and is a function of the die size, as shown in Figure 8. This is due to improved optimization of die-stepping algorithms to maximize the number of full die. Larger diameter wafers also allow a reduction of the number of partial die around the perimeter of the wafer; this effect is more dominant for larger die sizes. Manufacturing on larger diameter wafers offers an improved economy of scale.

The use of larger diameter wafers does increase wafer cost. However, we will show that there is a reduction in the die cost. Early on in the introduction of a new wafer size, a 70% increase in wafer cost is reasonable[4]. In mature production the cost to process a larger diameter wafer could increase 30%.

Relative Die Cost on larger diameter wafers = W/g,

where W is the relative wafer cost for the larger wafer and g is the relative GDPW

As mentioned earlier, the range of values for W are 1.3-1.7 and for g are 1.8-2.5. Therefore, the range of relative die cost is 0.5-0.9, a 10-50% die cost reduction when using larger diameter wafers.

A couple of examples for a mature and a relatively new technology are shown here:

a. For a 10mm die in 0.8um technology processed on 150mm and 200mm wafers, W=1.35, g=1.95. Therefore, die cost on 200mm wafers = 69% of die cost on 150mm wafers.
b. For a 10mm die in 130nm technology processed on 200mm and 300mm wafers, W=1.75, g=2.45. Therefore, die cost on 300mm wafers = 71% of die cost on 200mm wafers.

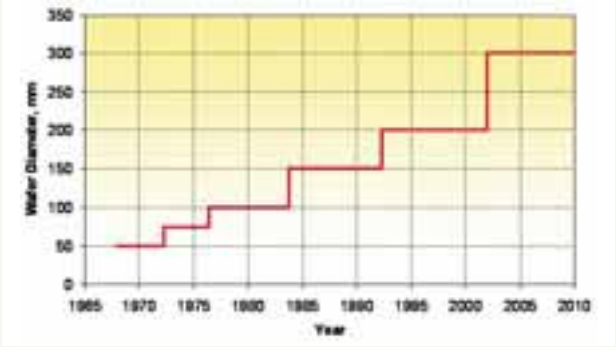

Figure 6 Silicon wafer diameter increase over time

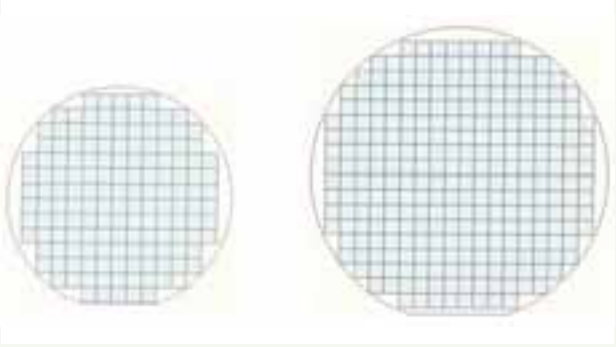

Figure 7 Increased gross die from a wafer diameter increase in the same technology

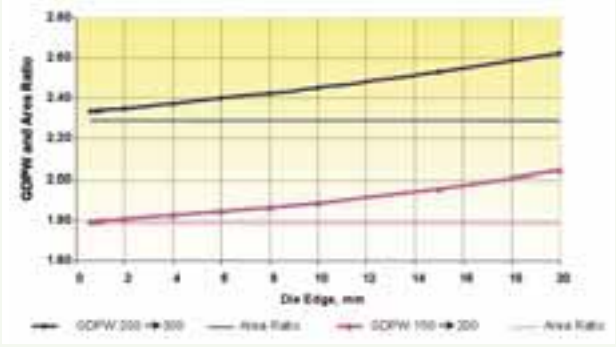

Figure 8 GDPW increase as a function of die size for two different wafer size transitions

6. Optimizing the Die Size and Packing Density per Chip

Selecting the optimum packing density and the die size becomes a challenge in this dynamic industry. We have developed models to predict the optimum die size and functions per chip. In Figures 9 and 10 we show examples of the cost/gate for 90nm and 180nm technologies as a function of die size and millions of gates per chip. The curves have a U-shape. If the die size is too small the cost is dominated by the

overhead of the input/output structures, the scribe lane, etc. If the die size gets too big, the cost per gate increases due to the increased complexity. For simplicity, gate count is assumed here to be an equivalent 2-input NAND gate count. Each equivalent gate uses four transistors. The optimum gate density and cost per gate can be converted to transistor density and cost per transistor. The actual transistor count per chip increases rapidly as larger amounts of memory is included on the die. For reference, one of Intel's Pentium processors is reported with 55M transistors (14M equivalent gates) in a 90nm technology[4]. Referring to Figure 10, this data point will be considered reasonably well optimized in our analysis, since it is located near the minimum, just at the cusp of the steep slope and marked by the arrow. The shape of the curve is affected by parameters such as wafer cost, defect density, physical and electrical design rules, design tools' packing efficiency.

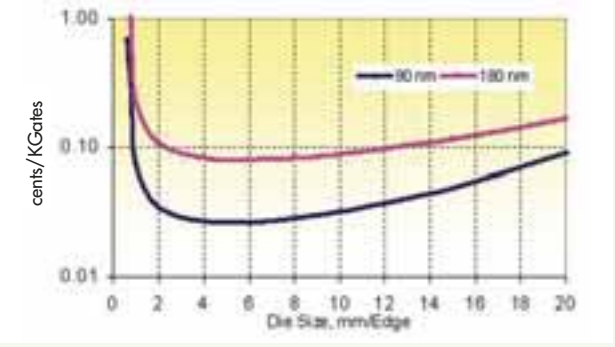

Figure 9 Cost per gate as a function of die size for 90nm and 180nm technologies

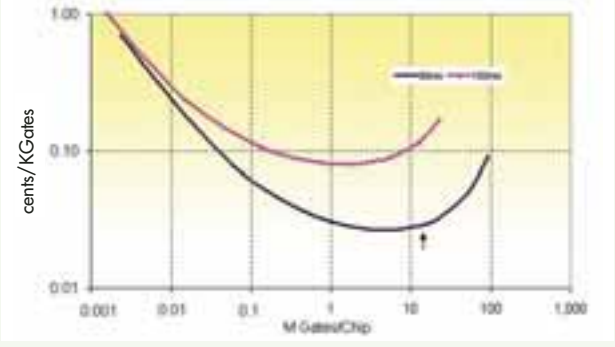

Figure 10 Cost per gate as a function of packing density for 90nm and 180nm technologies

7. Current Trends

This paper has focused on providing a historical perspective of business aspects of scaling. While a detailed discussion of the current status of technical and business challenges is beyond the scope of this paper, we will provide some highlights of current trends in this section.

a. The cost of wafer fabrication facilities and equipment, masks and chip design have all escalated significantly over the years. Finding solutions to technical challenges at the 32nm node will require ever increasing capital and manpower investments.
b. Manufacturing entities have worked diligently to accelerate the manufacturing and defectivity learning curves.
c. Creative co-design of process and design considerations has been called for by many authors[10] and are being implemented to manage challenges such as increased leakage and standby power.
d. New product introductions on the 65nm technology node have been made at leading edge users in the 2005 time frame; the cross-over point varies but is expected to be in 2007. Lead products on 45nm will likely be announced in 2007 with a cross-over in 2009. These timetables indicate a less than 3 year cycle for the introduction of new technology nodes.
e. As in the past, technical solutions for the next technology (32nm), e.g. the use of double-exposure lithography, will add significantly to capital, process development and therefore wafer cost. The author is confident that the industry will find a new manufacturing and design optimization point that will allow introduction of new products cost-effectively at this node.
f. The increasing cost of wafers, masks and design require users to very carefully assess the selection of the proper technology for their products. The trend is towards the use of leading edge technology nodes only for products with very high volumes, a compelling technical argument and a clear value proposition.

8. Summary

This paper has provided a simplified view of the business aspects of scaling and technology migrations that have been key to sustaining a phenomenal reduction in CPF for integrated circuits. Although trends such as the increasing cost of wafer fabs, masks and the increasing cost of complex designs indicate a possible slow down of the implementation of new technologies, the industry marches onward. The industry has demonstrated resilience in finding solutions to challenges. New technologies are still being introduced at a feverish pace allowing increased packing density, reduced CPF and improvements in performance.

9. Acknowledgements

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A Perspective on the Theory of MOSFET Scaling and its Impact

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It was certainly the best of times to work on silicon integrated-circuit technology when I joined IBM Research in 1973. My first assignment was to study the so-called hot-electron effects in MOSFET's. At the time and for many years that followed, hot-electron effects severely limited the progress of MOSFET technology, particularly CMOS technology. The reasons for this will be explained later. In the subsequent three decades, I have had the opportunity to participate in the evolution of silicon integrated-circuit technology and witness the tremendously rapid rise and fall of a couple of the platform technologies. One of the most significant milestone events along the way was the establishment of a theory for scaling down the physical dimensions of MOSFET's, published in 1974 [1]. In this paper, I provide a brief personal perspective on the significant role this theory played in the evolution of silicon integrated-circuit technology.

From the very beginning, the basic idea of integrated-circuit technology has been to employ advanced lithographic and process techniques to make ever smaller devices and to increase the chip-level integration. The technology to produce stable n-channel MOSFET's was developed in IBM in the 1960's [2]. Using n-channel instead of p-channel, the performance of MOSFET's was improved by about a factor of two. In 1963, CMOS circuits were reported with the promise of negligible standby power dissipation [3]. So, when the theory of MOSFET scaling [1] was published, the prospect of MOSFET circuits with very low standby power dissipation, that are both simple to make and scaleable, seemed quite realizable. The theory prescribed some simple rules to follow in scaling and described the expected resultant circuit benefits, as listed in Table I. To first order, the expected drain current equation for the scaled MOSFET is given by

$$I_d(\text{scaled}) = \frac{\mu_{eff}\varepsilon_{ox}}{t_{ox}/\kappa}\left(\frac{W/\kappa}{L/\kappa}\right)\left(\frac{V_g - V_t - V_d/2}{\kappa}\right)(V_d/\kappa) = \frac{I_d(\text{reference})}{\kappa} \quad (1)$$

where I_d (reference) is the drain current of the reference MOSFET and I_d (scaled) is the drain current of the scaled MOSFET.

TABLE I: Rules and results for circuit performance in scaling MOSFET by a factor κ [1]

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time per circuit VC/I	$1/\kappa$
Power dissipation per circuit VI	$1/\kappa^2$
Power density VI/A	1

However, a typical MOSFET in production in the early 1970's had a gate oxide of about 100 nm in thickness, a channel length of about 5 μm, and a power supply voltage of 5 V or larger. As explained in a paragraph below, the performance of these high-voltage MOSFET circuits was simply much too inferior compared to the performance of silicon bipolar circuits. Bipolar was the high-performance technology, the backbone of computers and high-performance electronics, while MOSFET was the low-cost technology for applications where performance was not required.

The benefit of applying the scaling theory to MOSFET technology, especially to CMOS technology, seemed obvious and exciting. If we just follow the rules and scale the CMOS devices by a factor of ten, the resulting circuits will be ten times faster. For more than two decades following the publication of the MOSFET scaling theory, CMOS engineers focused much of their efforts in scaling down the physical size of CMOS transistors. However, instead of scaling down the power supply voltage, they left it at 5 volts, which was the standard for practically all integrated circuits. There was simply little or no market for integrated-circuit chips using non-standard voltages. Such constant-voltage scaling of MOSFET quickly ran into two major difficulties, namely the power density of a CMOS circuit in switching increased very rapidly by a factor of κ^2 to κ^3, and the fast increasing electric field caused hot-electron and oxide reliability problems. Power density was not much of a problem because the integration level was still relatively low so that the total chip power was readily manageable. However, device engineers had to devote much effort to develop practical techniques, such as LDD (Lightly Doped Drain) [4], in order to bring the reliability issues under control. Controlling hot-electron effects added significant cost to the CMOS chips.

Scaling at constant voltage severely limited the performance potential of CMOS as well, particularly for driving long wires and driving signals off chip. To first order, the performance for driving a capacitance load C is CV/I, where V is the voltage swing and I is the current delivered by the transistor. For bipolar circuits, V is typically about 200-400 mV for driving on chip, and about 800 mV for driving off chip. Thus, at 5 V, the voltage swing of CMOS circuits was much too large for high-performance applications. Besides, in the late 1970's, bipolar engineers also developed a theory for scaling bipolar circuits [5] which guided the rapid development of faster and lower-power bipolar circuits. For more than twenty years after the MOSFET theory was published, CMOS remained a low-cost technology limited to applications where performance was not an important factor. When performance was needed, scaled advanced bipolar technology was used.

The opportunity for scaled CMOS to break into high-end applications came when the industry worked together to established voltage standards below 5 volt. Once it was recognized that CMOS at less than 5 V could be accepted by the market, engineers wanted to reduce CMOS voltage as fast as possible. As an illustration of this "lower is better" mind set at the time regarding CMOS voltage, Figure 1 is a plot of three CMOS voltage roadmaps proposed in the early and mid 1990's. At the first semiconductor technology roadmap workshop in 1992 [6], there was a consensus that CMOS power supply voltage would not be below 2 V until 2004. In 1995, it was proposed that leading CMOS should have a power supply voltage of 1.8 V in 1999. By the time the 1997 roadmap [7] was prepared, it was proposed that the voltage in 1999 should be 1.5 V instead. For several years now, advanced CMOS microprocessor chips use a power supply voltage of 1 to 1.2 V.

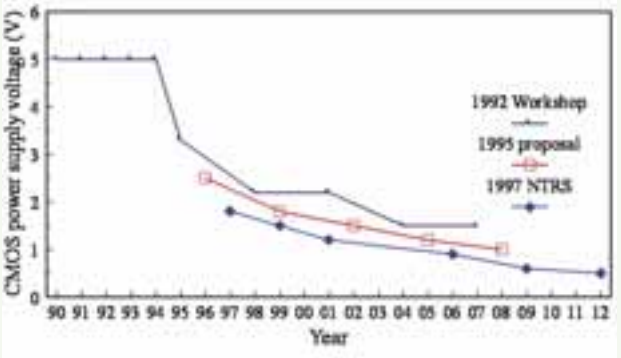

Fig. 1. Proposed power supply voltage trends for CMOS. (After references [6] and [7])

Reducing CMOS voltage makes the fabrication process for scaled CMOS less complex and hence lowers the cost. For one thing, process steps used to implement LDD can be omitted. With the introduction of scaleable technology elements such as shallow-trench isolation and dual-poly gate (i.e., p+-polysilicon gate for p-FET and n+-polysilicon gate for n-FET) to the fabrication of reduced-voltage CMOS circuits, as illustrated in Fig. 2, CMOS technology became readily scaleable [8]. The same device schematic in Fig. 2 was used to represent several generations of CMOS technology, making the migration of devices and circuits from one generation to the next relatively simple to implement, and exhibited more predictable results. For the decade that followed, there was accelerated progress throughout the semiconductor industry scaling such a CMOS device structure to ever smaller dimensions, as evidenced by the accelerated rate at which CMOS power supply voltage was reduced.

With CMOS channel lengths scaled to around 100 nm and voltages reduced to around 1 volt, the performance of digital CMOS became comparable to that

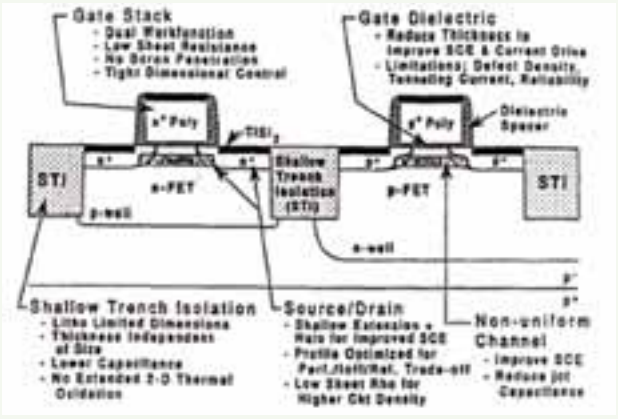

Fig. 2. Schematic of a CMOS device structure that was scaleable to deep sub-micron dimensions. (After Davari, [8])

of digital bipolar. The era of bipolar for high-performance digital circuits came to an end when IBM decided to replace bipolar by CMOS as the technology for mainframe computers. At first, the CMOS mainframe processors was not really as fast as the bipolar versions, but the highly scaleable properties of CMOS allowed CMOS processors to catch up in just a few years, as shown in Fig. 3 [9]. Since then, CMOS has become unquestionably *the* technology for all digital applications.

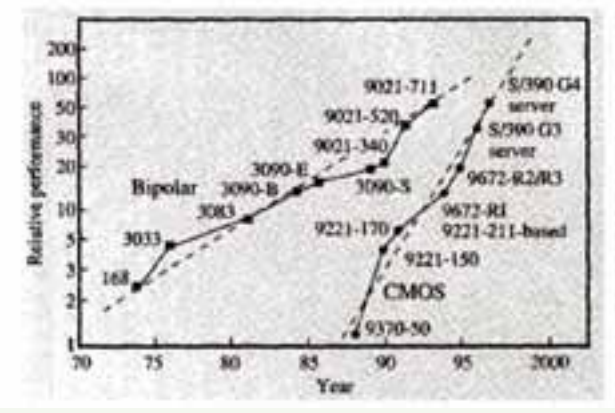

Fig. 3. IBM S/390 mainframe uniprocessor performance. (After Rao et al., [9])

Every technology has its limits, and CMOS is no exception. The fact that the CMOS device structure depicted in Fig. 2 is highly scaleable was both good news and bad news. The good news was that it became relatively straight forward to establish an industry-wide technology roadmap, and every leading semiconductor company wanted and was able to beat the roadmap targets. Again, this is evidenced by the increasingly aggressive rate of CMOS power supply voltage reduction illustrated in Fig. 1. System developers and consumers certainly benefited tremendously from the faster-than-projected rate of CMOS scaling. The bad news was that the industry also reached the limits of CMOS scaling at rate faster than anticipated.

Two of the limits of CMOS scaling were reached in the early 2000's. These limits are the high tunneling current through the thin gate insulator and the high device off current. That we reached these scaling limits so soon should come as no surprise. In the case of gate insulator thickness, it was shown that scaling CMOS to the regime where gate tunneling current is appreciable has little impact on the device characteristics [10]. Today, leading-edge CMOS microprocessor chips employ gate oxide layers as thin as 1 nm, which is pretty much the limit set by acceptable gate tunneling current. The limit due to high device off current has been looming there since the very beginning, as shown in Eq. (1). In Eq. (1), the factor $[V_g - V_t - V_d/2]/\kappa$ scales only if the threshold voltage V_t is scaled. If V_t is not scaled, this factor is smaller than expected from scaling and the resultant device speed is less than expected from scaling. As the CMOS voltage was scaled below about 2 V, device designers had to reduce V_t in order to achieve the intended device performance targets. Reducing V_t has the effect of increasing the device off current, as illustrated schematically in Fig. 4. Reducing V_t repeatedly for several generations has lead to a dramatic increase of CMOS device off current. Today, CMOS circuits no longer have negligible standby power dissipation. Instead, the performance of leading-edge CMOS logic chips is limited by a combination of device off current and gate tunneling current.

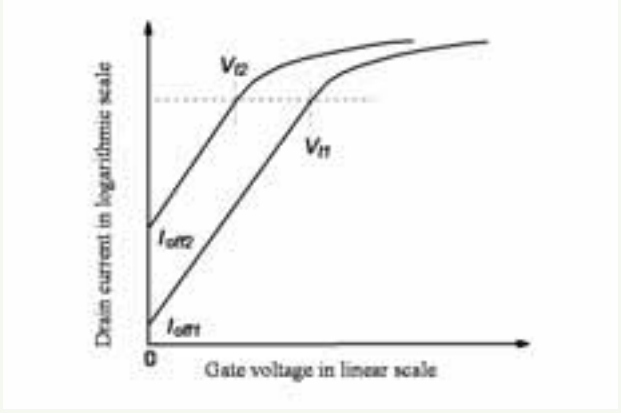

Fig. 4. Schematic showing the increase of device off current when V_t is reduced, where $V_{t2} < V_{t1}$.

Without the ability to reduce gate insulator thickness and device threshold voltage any further, CMOS device designers find it difficult to increase device speed by the usual means of scaling device channel length. Today, device engineers focus primarily on technology innovations for continued device performance improvement from one generation to the next. The most notable innovations that have been successfully developed and put into volume manufacturing to date include using silicon-on-insulator (SOI) as the wafer substrate [11], using embedded SiGe in the source/drain region of p-channel FET's to improve hole mobility [12], and using highly-stressed dielectric films on top of n-channel FET's to improve electron mobility [13]. Each of these innovations offers incremental but appreciable improvements to the

speed and/or power dissipation of CMOS circuits. Circuit designers can always tradeoff the speed improvement for lower power dissipation. Judging from the presentations at device conferences, it is reasonable to expect a steady stream of additional innovations for enhancing CMOS performance to become ready for manufacturing in the next decade.

Nowadays, the concern is not the lack of innovative ideas for improving CMOS performance, but the time and cost needed to bring a specific innovation from its concept stage to volume manufacturing. Most major innovations take 10 ±5 years from concept to manufacturing, which is long compared to the 2 to 3 years to scale CMOS from one generation to the next (the linear dimension is reduced by a factor of 0.7 and the circuit density is improved by a factor of 2 each generation). Going forward, it is important that circuit and system designers recognize this paradigm shift in CMOS development and plan their product strategies accordingly.

Thanks to the insights provided by the simple theory of MOSFET scaling, we have been able to make unprecedented progress in advancing CMOS technology over a period of about thirty years. In the process, we have run the course of CMOS development guided by the theory of scaling. We have left the period when leadership in CMOS technology was judged by being the first to scale CMOS to the next dimensional node and entered a period when leadership is judged more by being able to enhance chip-level performance through innovation.

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[13] Most dielectric films are of high stress as deposited. Until recently, device engineers worked hard to minimize the stress in the deposited films to avoid possible deleterious effects such as wafer bowing and film cracking and/or peeling. To day, device engineers work hard to increase the stress in a controllable manner to increase n-FET drive current.

About the Author

Tak H. Ning received his Ph. D. degree in physics from the University of Illinois at Urbana-Champaign in 1971. He joined IBM Thomas J. Watson Research Center in 1973. His early technical contributions were in understanding hot-electron effects and in advanced bipolar technology. From 1982 to 1991, he managed the silicon devices and technology department in IBM Research, contributing to and leading the research effort on CMOS, bipolar, DRAM, EEPROM and SOI. He was appointed an IBM Fellow in 1991. In recent years, he has focused his technical activities on understanding the limits of CMOS as well as the opportunities beyond CMOS. He received the 1989 IEEE Electron Devices Society J.J. Ebers Award and the 1991 IEEE Jack A. Morton Award. He is a member of the National Academy of Engineering, and a fellow of the IEEE and of the American Physical Society.

Impact Of Scaling and the Scaling Development Environment

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The largest question in the early to mid 70's was how far silicon could go in competition against newly emerging materials and devices such as magnetic bubble memory, Gunn effect functional devices, integrated injection logic, GaAs MESFET integrated circuits, and Josephson junction logic.

The typical roadmap of major semiconductor manufacturing companies in those days was such that (1)Silicon based integrated circuits would lose position by the mid 80's except for silicon on sapphire, SOS, based ones, (2)GaAs integrated circuits would become the dominant design for high speed and /or low power applications, (3) Optical lithography would surrender its position against either electron beam lithography or soft X-ray lithography, (4) Geometry shrink, however, may proceed despite challenges around. In other words, no one was even close to predicting what we are seeing today. In fact, many central research organizations in industry decided that silicon would not be a right subject any more for advanced research, and either shut down silicon research activities or transferred the division to their operation divisions.

In the middle of the 70's, Japan launched a large national project, called the "VLSI project" which was instigated by the announcements made by Bell Laboratories for electron beam direct writing lithography, and by IBM demonstrating 8kbit dynamic random access memory at 1um minimum geometry, both of which were supposed to provide solutions for future computing systems in the mid 80's and beyond. The project consisted of Fujitsu, Hitachi, Mitsubishi, NEC and Toshiba, and had a centralized research center for basic research to which all member companies sent researchers, and also two branch laboratories for Fujitsu-Hitachi-Mitsubishi group and NEC-Toshiba group focused on more development oriented work. Two government laboratories, Electrotechnical Laboratory and NTT Laboratories were also involved.

Moore's Law was already becoming popular, but when it came to any methodical approach to make it happen rather than a religious belief, there was not much idea which was viewed credible enough. Japan's VLSI project had both logic and memory as the targeted areas with MOSFETs, bipolar such as ECL/CML, and compound semiconductor devices. The tool side was even broader, covering from optical, electron beam and X-ray lithography, plasma processes and a variety of thermal processes. This almost implied that we needed to look around for 360 degree instead of any particular focus. Also, it was the time when layout design was viewed as such a serious bottle neck that almost 90% of the world population might need to become layout designers and technicians by the end of the 80's. Fortunately, many IEEE technical conferences, such as IEDM and ISSCC were quite interesting in terms of a large variety of research results presented, but when it came to the future of silicon integrated circuits, general perception was to seriously stagnant at around 1um geometry.

Dr. Robert Dennard's paper in 1974(1) appeared in the IEEE Journal of Solid State-Circuits. As the first proposal for the scaling principle, it looked, at first glance, rather simple and did not attract much attention, at least I remember from a little corner of Toshiba Research and Development Center where I was in charge of SOS microprocessor technology and also involved in Japan's VLSI project looking into short channel MOSFET technology research. However, it did not last long before more people started understanding what it possibly would imply to the world of MOS integrated circuits. However, it needed to wait for CMOS taking the "dominant" design position in the mainstream of integrated circuits before the scaling theory became the physics based guiding principle for Moore's Law to continue. Without scaling theory, I doubt that Moore's Law could have survived for more than three decades. It was the first attempt to couple geometry shrink with other important factors such as power-delay products, on-chip interconnect performance as well as integration density. The magic number alpha of "1.4" or 0.7x shrink over all device parameters, as shown below became a general guideline from one technology node to the next technology node since then.

dimensions tox, L, W	$1/\alpha$
doping	α
voltage	$1/\alpha$
integration density	α^2
delay	$1/\alpha^2$
power dissipation/Tr	$1/\alpha^2$

It is indeed difficult to see any other such example in which one set of rather simple principles can survive for such a long time. I would, however, say

that this has survived because of its simplicity and transparency. There have been enormous impacts coming from the scaling principle, not only in the way we design devices and develop technology to meet requirements, but also on the semiconductor device manufacturing industry as well as manufacturing equipment business by providing clear and easily understandable directions with investment timing. The scaling principle and Moore's Law have been inseparable in terms of providing a driving force to technology research and development and justifying huge investment for more advanced infrastructures for manufacturing. It was because scaling continuously provided 2x density of integration at reduced cost per gate or bit with better performances to integrated circuits chips designed and manufactured with more advanced technology in the past three decades. It should not be forgotten that scalable design library has become one of the prerequisites for the design community, which cut down design cost increase coupled with enormous progress made in computer aided design from logic design down to layout design capability.

Today we are still thinking with the scaling principle even though the scaling factor could be quantized due to actual size approaching the integer times an atomic size, and performance would be in the same way as somewhat quantized by nature. This would force us to rethink scaling not just for the geometry scaling, but also consider a variety of new materials to keep the pace of improvement both in performance and cost. As we see the era for "nanoelectronics" either evolutionary and/or revolutionary challenges, this is a great moment at which we all should appreciate what Dr. Dennard has given to all of us.

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About the Author

Yoshio Nishi is a Professor in the Department of Electrical Engineering (research) and in the Department of Material Science and Engineering at Stanford University He also serves as Director of Stanford Nanofabrication Facility of National Nanotechnology Infrastructure Network of US, and Director of Research of Center for Integrated Systems.

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He moved to Hewlett-Packard in 1986 as the Director of Silicon Process Lab, followed by establishing ULSI Research Lab as the Founding Director.

In 1995 he joined Texas Instruments, Inc as Senior VP and Director of Research and Development for semiconductor group, and implemented new R&D model for silicon technology development, followed by establishing the Kilby Center.

In May, 2002, he became a faculty member of Stanford University. His research interests cover nanoelectronic devices and materials including metal gate/high k MOS, device layer transfer for 3D integration, nanowire devices and resistance change non-volatile memory materials and devices. He published more than 200 papers including conference proceedings, and co-authored/edited 9 books. He holds more than 70 patents in the US and Japan.

During the period of 1995-2002 he served SRC and International Sematech as Board member, NNI Panel, MARCO Governing Council. etc. Currently he is an associate member of the Science Council of Japan.

Dr. Nishi is a Fellow of IEEE, a member of Japan Society of Applied Physics and the Electrochemical Society. Recent awards include the 1995 IEEE Jack Morton Award, and the 2002 IEEE Robert Noyce Medal.

It's All About Scale

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Abstract

The electronics industry often thinks of scaling in only one dimension: making things smaller. But it really scales in two directions, both smaller and larger, and the semiconductor industry has employed both, allowing roughly 40 years of exponential progress in the cost reduction of electronic functions. The future of the semiconductor industry holds daunting challenges, including some related to scaling things larger, but a historical view shows this has always been true.

Introduction

The topic of scaling usually invokes pictures of ever smaller features, transistors and wires, packing ever more functions onto densely packed circuit boards. On the other hand, fabs, tools, teams and complexity have been increasing in size at nearly the same exponential pace. It is the combined effect of these two trends, smaller features working to solve larger problems, that has allowed rooms full of electronic equipment to shrink into slivers of silicon, at a fraction of the cost, operating at a fraction of the power, and available to anyone, anywhere in the world. However, just as the amount of silicon required to perform a function has gotten smaller, the number of users and their demands has scaled up. A modern data center is capable of serving millions instead of few, and of solving bigger problems with ever greater precision.

Looking back at the progress of integrated circuit scaling, it is easy to forget that it was never obvious how to progress beyond the next two generations. The few that tried to extrapolate progress beyond this window, or proclaimed that the end of scaling was near, were mostly proven wrong. With that historical lesson in mind, the following sections look at the recent past and near term future of feature scaling, resource scaling, and application scaling.

Scaling Transistors and Interconnect

Insights into the scalability of the physics of field effect devices unleashed a steady and rapid reduction in feature sizes. Under conditions of constant electric fields, smaller devices switch faster at lower power. Density increases quadratic, power dissipation reduces cubic, and speed increases linearly. Ideally then, scaling allows more things to happen faster at the same energy cost, and is economically attractive if the manufacturing cost per square area grows only modestly. Specifically, in the past decade or so, CMOS has improved density at each node by 2x, increased performance more than 20%, while limiting increases in the final cost per wafer to less than 30%. The compound effect of a new node every two (early on, three) years has brought mainframe capability down to the package of a cell phone. We've moved from megawatts to milliwatts, from MHz to GHz, from kilobits to gigabits, and so on. Most importantly, all while moving from millions of dollars to just a few dollars .

This progress wasn't obvious at the outset. If we had known then what is possible now, we would have done it faster. Every time a new node is contemplated, lithography capability is two generations away from physical or practical (i.e. economic) limits. Today, the patterning process calls for 193nm immersion lithography with various resolution enhancements. Combining wavelength reduction, lens improvement, mask sophistication and resist enhancement now allows printing of features with a minimum pitch of lines and spaces near 125nm. Future improvements in numerical aperture (NA) to 1.35 are expected to bring this down to sub-80nm for regular arrays. Printing even smaller features with higher transistor density may require new capability such as Extreme UV, which requires all reflective optics and a vacuum toolset. Serious challenges also need to be overcome with regard to source power and mask capability. The perennial alternative, direct-write e-beam, may have application in very low volume product or as mask writer, using a massively parallel beam to overcome the charge-throughput limitations of a single beam. In all cases, the mask plays a critical role, and has become the key concern for designers.

Masks are no longer "black and white" but their features manipulate a complex two-dimensional contrast image through focus and exposure windows. This specialty of Resolution Enhancement Technology (RET) has resulted in tricks like Sub Resolution Assist Features (SRAFs) for vias, model-based Optical Proximity Correction (OPC), and will likely embrace model-based placement for SRAFs and dual-pattern, dual-etch for better poly and contacts definition. As one might imagine, these techniques have greatly contributed to the cost of masks, and hence product design. Scaling down has meant scaling up.

While the horizontal dimensions have become smaller than the gate dielectric of the past, the technology has reached the practical limits of oxide thickness reduction. While dielectric improvements using Nitrogen and/or Hafnium may extend the effective thickness, it is likely limited to at most a factor of two. Additional benefits may be gained

from metal gate electrodes by eliminating the depletion layer on the top side of the dielectric. Any mobility degradation because of additional scattering will be overcome by the significant mobility enhancements due to strain. In fact, the successful application of strain is a superb example of unanticipated improvements that work precisely because of the new small scale of the devices. Many of the effects below 100nm introduce problematic behaviors: tunneling contributes to leakage in thin dielectrics and high field junction profiles; line edge roughness in resists patterns results in excessive short channel effects; and grain–boundary and sidewall scattering increase the resistivity of copper wires with very small cross-sections. Low resistance is critical to high efficiency use of the device properties. Contact and via resistance are therefore becoming a bigger concern going forward as their properties scale non-linearly in the wrong direction. And, as many now know, the capacitance of the interconnect is approaching its physical limits as well. The low dielectric constant materials that reduce the k-value from 4 for silicon dioxide, to around 2.5 for heavily Carbon mixed compounds, are mechanically weak and can interfere with packaging robustness, as well as cause electrically lower breakdown voltages.

All these process and materials changes have allowed density scaling to continue at its historical pace of 2x every generation. The price has not only been more complexity, but also the introduction of several design tradeoffs. Design innovations now need to limit static and dynamic power dissipation, tolerate escalating parameter variations, maximize increasingly restricted layout options, and incorporate analog and RF functions at the low voltages compatible with extremely small dimensions.

Scaling the Resources

Immersion lithography allows for effectively shorter wavelength and a higher NA lens design to improve the lithographic patterning pitch. A manufacturable implementation requires cost effective throughput, defect density, and resist solution. The large increase in capital equipment cost consumes the largest fraction of the process cost budget. As is the case for every process tool, to maintain cost effectiveness, high throughput/automation is required to offset the initial capital outlays. But now the high volume capability of each tool requires the fabs to be ever larger to avoid one-of-a-kind tool challenges. In addition, chips now may include over 10 layers of interconnect. While the process is repeatable, the interconnect fraction of a fab is easily half the fab size because of the multitude of tools. The explosion in process steps, represented typically by the number of mask layers has also increased rapidly. The size and cost of fabs has thus grown exponentially, each supplying an ever larger fraction of the market, and each generation requiring a larger investment and higher market risk.

Resource demands have also rapidly grown on the product side. Thanks to the ability to yield hundreds of millions of transistors on a single die, design teams for chips are now equivalent to those that were required to build large computers. Product designs need to comprehend everything from knowing the strengths and limitations of the process, to defining and building the software infrastructure that support such sophisticated systems-on-a-chip.

Scaling the Applications

Absolute interconnect performance has become a dominant speed limit and, consequently, variations in line-width and thickness add increasingly to the design margin. While many effects are systematic, the complexity of interconnect prevents a brute force computational solution. This has become typical of the technical problems to be solved at the design and application level. Conceptually, the problem of optimizing interconnects to minimize delay and power is governed by simple physics. However, the sheer size of a problem like this, or that of RET or for that matter, fab operations, is overwhelming. Not just for the design teams, but frequently for their compute resources as well. And finally, the challenge is not overcome by solving a steady state or exact condition. Parameters are not perfectly controlled, and it is becomingly increasingly clear that comprehending variations is where the next breakthrough may be needed. Nature gives us examples of how it has figured out that designing with imperfect and infinitely variable components can be successful. Although human communication may be effective while being imperfect, other communication or computation tasks cannot tolerate any practical errors.

For example, encouraging progress by the EDA tool suppliers is trailing the needs for leading product designs. Integrating analog and RF functions in advanced CMOS requires an architectural approach to maximize the features of density and speed, rather than the precision of analog components.

Summary

Over the past 40 years the world has benefited from exponential growth in the application of semiconductors. Thanks to scaling transistor dimensions into the nanometer regime and scaling the manufacturing capabilities to produce billions of individual chips, the industry has achieved economies of scale that allow what was once mainframe capability to be affordable to everyone in the world in something as small as a

cell phone. With many fundamental physical scaling limits still far away, this progress can and will continue if demand for the applications supports the increased investment necessary to get there.

About the Author

Johannes M.C. (Hans) Stork is Senior Vice President and Chief Technology Officer of Texas Instruments Incorporated. As Director of the Silicon Technology Development organization, Dr. Stork's primary responsibilities are the development of advanced CMOS, packaging and mixed signal process technologies.

He joined Texas Instruments in September 2001, after being the Director of the Internet Systems and Storage Lab at HP Laboratories, Hewlett-Packard from 1999 until 2001. He had joined Hewlett-Packard in 1994, holding the position of Director of the ULSI Research Lab between 1995 and 1999.

Dr. Stork started his professional career in 1982 at IBM's T.J. Watson Research Center as a research staff member in the bipolar technology and circuits area. Starting in 1987 he led an exploratory devices group which demonstrated record breaking SiGe HBTs. Hans was awarded two Outstanding Technical Achievement Awards from IBM. He has written or co-authored nearly 100 cited papers and holds eleven US patents. He was elected IEEE Fellow in 1994 for his contributions to SiGe devices and technology.

Hans has served on various conference and IEEE committees, including IEDM, VLSI, and BCTM between 1986 and 1996. Presently, Dr. Stork serves on the Board of Directors of Sematech, and is chairman of the Semiconductor Research Corporation (SRC) Board of Directors. He has been a member of the SIA Technology Strategy Committee since 1999.

In 2000-2001, he participated as a technical advisor to Government efforts on high performance computing benchmarks and the national security issues of Internet computing, and has recently been elected a member of the advisory committee for the Emerging Technology Fund in the state of Texas.

Dr. Stork was born in Soest, The Netherlands, and received the Ingenieur degree in electrical engineering from Delft University of Technology, Delft, The Netherlands, and holds a PhD from Stanford University.

These three reprints show the difference between conference and journal reporting in the 1970s. When the concept of scaling first saw the light of day at IEDM in 1972, only an abstract remained as an archive report. By 1973, the IEDM Digest provided a broader basic overview of Dennard's report. Denard's 1974 explanation of scaling turned out to be the most cited article in the 51 year history of the JSSC, close to 700 times, according to the last count in 2005 by the independent citation report firm, Thomson ISI (sscs.org/jssc/topcites.htm). The mission of Journal of Solid-State Circuits is to provide the full archival source for important technical milestones and fundamental explanations critical to the field.

Design of Micron MOS Switching Devices

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Modern photolithographic technology offers the capability of fabricating MOSFET devices of micron dimensions and less. It is by no means obvious that such small devices can be designed with suitable electrical characteristics for LSI switching applications. In this talk we will describe short-channel devices (L_{eff} ~ 1 μ) designed by scaling down larger devices with desirable electrical characteristics. Lateral and vertical dimensions, doping level, and operating voltages and currents are scaled in a self-consistent fashion. In this way small devices have been fabricated without the usual deleterious effects associated with short channels. The measured characteristics of these short-channel devices and the larger devices from which they were scaled will be compared.

The scaling procedure helps to better understand the limitations of miniaturization of MOS devices. Significant problems are encountered when operating voltages become comparable to the band gap which cannot be scaled within the silicon technology. The subthreshold characteristic of the device then becomes an important consideration.

Ion Implanted MOSFET's With Very Short Channel Lengths

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It has been shown previously that MOSFET switching devices can be scaled down to have one micron spacing between source and drain. In order to achieve electrical characteristics suitable for dynamic memory and other digital applications, such miniaturized devices must have reduced gate insulator thickness and junction depth, reduced operating voltages, and increased substrate doping (1). The previously described one micron device structure is shown in Fig.1(a). With uniform substrate doping, a 200°A gate insulator is required to achieve the desired control of the gate threshold voltage over the operating range of the source and drain voltages.

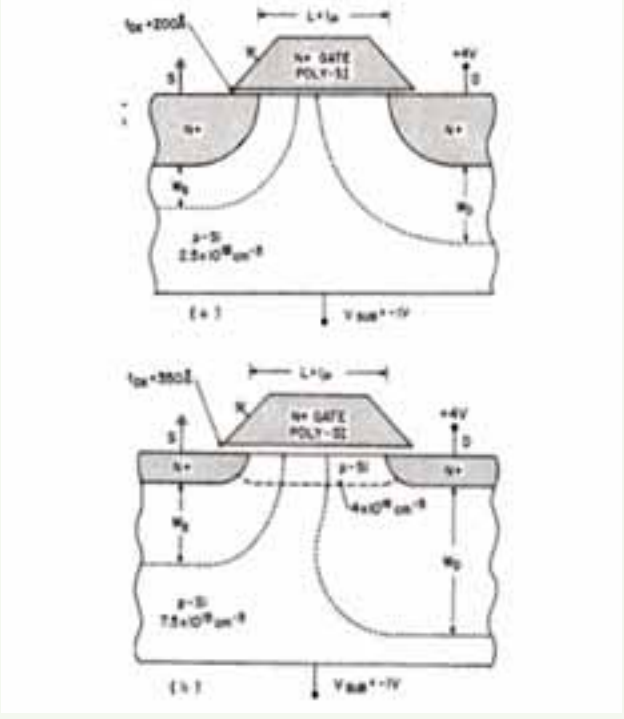

Figure 1: MOS device designs for micron source-drain spacing. (a) Unimplanted design (b)Design with ion implantation.

The present paper addresses improvements in the design of micron devices which can be obtained by using ion implantation. The new n-channel design, which is shown in Fig. 1(b), uses a lighter doped substrate with a relatively heavy doped p-type region at the surface between the source and drain. This implanted p-type region gives the desired threshold magnitude, and also controls the extent of the source and drain depletion regions beneath the gate. With the gate turned off, these depletion regions must be kept separated so that the surface potential in the channel region is indeed controlled by the gate. Merging of the depletion layers in the lighter doped substrate is prevented by using shallow implanted source and drain junctions of depth comparable to the p-type implanted region, and also by choice of a moderate substrate doping level.

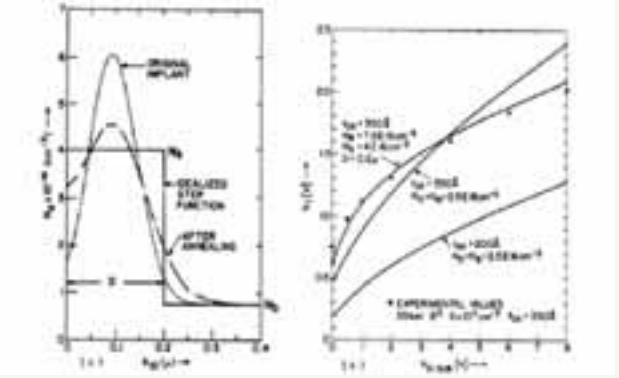

Figure 2(a) Vertical substrate doping profile, and (b) the resulting threshold versus source - substrate bias characteristic compared with alternate approaches. Experimental confirmation is shown by large dots.

The vertical-doping profile of the implanted region beneath the gate is shown in Fig. 2(a). Intuitively, it was felt that a step function profile is preferable for the one micron implanted device, and such a profile has been used for design purposes. In practice a single energy implant through the gate oxide with thermal treatment used in the subsequent processing gives a reasonably good approximation to the step function. Fig. 2(b) shows the gate threshold voltage (relative to the source) required to turn on the device as a function of the source - substrate potential using the one-dimensional model described in another conference paper (2). The implantation profile was chosen to be deep enough to prevent depletion layer punch through, and shallow enough to give the desired threshold voltage control with a 350°A gate insulator thickness. Throughout the operating bias range ($V_{s\text{-}sub} > 1$), the gate field for the threshold condition depletes the heavier doped implanted region, and this depletion extends well into the lighter doped substrate. This gives a threshold voltage relatively independent of source-substrate bias compared to a uniformly doped substrate with the same 350°A oxide thickness. (See Fig. 2(b)). Compared to a non-implanted design with a 200°A gate insulator, the new design has the same slope in the threshold versus source bias characteristic, but the overall threshold level is higher, which is desirable to provide adequate design margins for circuit applications.

The one-dimensional threshold model is adequate for devices with long source-drain separation, but in practice the short devices of interest suffer a decrease in threshold voltage due to penetration of the drain field into the channel region normally controlled by the gate. These short channel effects have been studied using a two-dimensional numerical model (3). The computed turn-on characteristic is shown in Fig. 3 for two values of source-drain spacing L in the range of one micron and for a relatively long (10 micron) device, all normalized to the same width-to-length ratio (W/L=1). A drain voltage of 4 volts is applied in all cases, which is the maximum considered for this design. The effect on the short devices is a shift of the characteristic along the gate voltage axis. This represents a lowering of the threshold voltage. (V_t corresponds to a drain current of about 10^{-7} amps above which the current varies as $(V_g-V_t)^2$ rather than exponentially with V_g. Otherwise the device turns off properly.

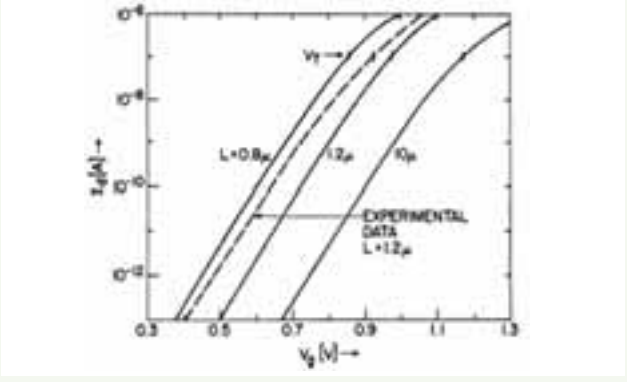

Figure 3: Computed and experimental turn-on characteristics for different values of source-drain spacing, L.

Experimental devices have been fabricated to test this design with various source-drain separations from 0.5 to 10 microns. The p-type region was obtained with a 35 KeV B^{11} implantation through the 350 Å gate oxide into 2 ohm-cm substrates. The narrow silicon gates were delineatead by contact printing from high-quality masks. Self-aligned source and drain regions were formed with a 100 KeV As^{75} implantation through the 350°A oxide layer. The most significant thermal treatment after the B^{11} implant was eleven minutes at 1000°C.

Good agreement was found between the threshold characteristics of the experimental devices and the design predictions as shown in Fig. 2(b). The turn on characteristic of an experimental device of L=1.2 microns displays the same behavior as the calculated characteristic. (See Fig. 3). The variation of threshold voltage with source-drain spacing (at maximum drain voltage) is shown in Fig.4 and compared with the calculated values from Fig. 3 (D=0.2μ).

Several design perturbations were simulated to test the sensitivity to key parameters. One variable which was investigated was the use of a shallower implanted surface layer, D=0.1 microns deep, with the dose adjusted to give about the same threshold value. Results for this case are also shown in Fig. 4. The shallower implant was found to be somewhat less effective in minimizing the threshold decrease for narrow source drain spacing. The sensitivity to the source and drain junction depth and to the background doping was also investigated, and the results are shown in Table I. These results show that there is little room for deviation from the original design and justify the original choices.

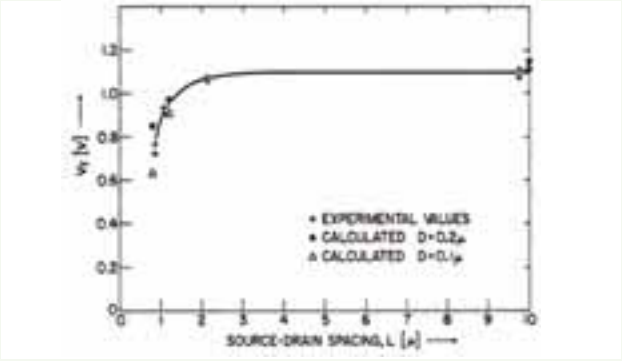

Figure 4. Experimental threshold voltage as a function of source-drain spacing compared to computed values.

Table 1

THRESHOLD VOLTAGE V_t FOR A DEVICE WITH 0.8μ SOURCE-DRAIN SPACING WITH VARIOUS DESIGN PERTURBATIONS (V_D=4 V, V_{sub}=-1 V)

Structure	V_t @ V_g (I_D=10^{-7}A)
Standard Design, D=0.2μ, X_j=0.2μ, N_B=7.3815e^{-3}	0.86 V.
Shallower Channel Doping, D=0.1μ	0.83 V.
Deeper Junctions, X_j=0.4μ	0.68 V.
Lighter Substrate Doping, N_B=1.3815 e^{-3}	0.54 V.

In summary, ion implantation allows the fabrication of very small MOSFET switching devices with considerably thicker gate insulators. Capacitance from the source and drain to the substrate and to the gate is reduced by more than a factor of two compared to conventional structures. Conversely, for a given thickness, smaller devices can be achieved using ion implantation.

Acknowledgements

We wish to acknowledge the valuable contributions of B.L. Crowder and F.F. Morehead, who provided the ion implantations and related design information. Also important were the contributions of P. Hwang and W. Chang to two-dimensional device computations. J. J. Walker and V. DiLonardo assisted with the mask preparation and testing activities. The devices were fabricated by staff of the silicon technology facility at the T.J. Watson Research Center.

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Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions

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Abstract—*This paper considers the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 μ. Scaling relationships are presented which show how a conventional MOSFET can be reduced in size. An improved small device structure is presented that uses ion implantation to provide shallow source and drain regions and a nonuniform substrate doping profile. One-dimensional models are used to predict the substrate doping profile and the corresponding threshold voltage versus source voltage characteristic. A two-dimensional current transport model is used to predict the relative degree of short-channel effects for different device parameter combinations. Polysilicon-gate MOSFET's with channel lengths as short as 0.5 μ were fabricated, and the device characteristics measured and compared with predicted values. The performance improvement expected from using these very small devices in highly miniaturized integrated circuits is projected.*

LIST OF SYMBOLS

α	Inverse semilogarithmic slope of sub-threshold characteristic.
D	Width of idealized step function profile for channel implant.
ΔW_f	Work function difference between gate and substrate.
$\epsilon_{si}, \epsilon_{ox}$	Dielectric constants for silicon and silicon dioxide.
I_d	Drain current.
k	Boltzmann's constant.
κ	Unitless scaling constant.
L	MOSFET channel length.
μ_{eff}	Effective surface mobility.
n_i	Intrinsic carrier concentration.
N_a	Substrate acceptor concentration.
Ψ_s	Band bending in silicon at the onset of strong inversion for zero substrate voltage.
Ψ_b	Built-in junction potential.
q	Charge on the electron.
Q_{eff}	Effective oxide charge.
t_{ox}	Gate oxide thickness.
T	Absolute temperature.
V_d, V_s, V_g, V_{sub}	Drain, source, gate and substrate voltages.
V_{ds}	Drain voltage relative to source.
V_{s-sub}	Source voltage relative to substrate.
V_t	Gate threshold voltage.
w_s, w_d	Source and drain depletion layer widths.
W	MOSFET channel width.

INTRODUCTION

New high resolution lithographic techniques for forming semiconductor integrated circuit patterns offer a decrease in linewidth of five to ten times over the optical contact masking approach which is commonly used in the semiconductor industry today. Of the new techniques, electron beam pattern writing has been widely used for experimental device fabrication [1]-[4] while X-ray lithography [5] and optical projection printing [6] have also exhibited high-resolution capability. Full realization of the benefits of these new high-resolution lithographic techniques requires the development of new device designs, technologies, and structures which can be optimized for very small dimensions.

This paper concerns the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1μ. It is known that reducing the source-to-drain spacing (i.e., the channel length) of an FET leads to undesirable changes in the device characteristics. These changes become significant when the depletion regions surrounding the source and drain extend over a large portion of the region in the silicon substrate under the gate electrode. For switching applications, the most undesirable 'short-channel" effect is a reduction in the gate threshold voltage at which the device turns on, which is aggravated by high drain voltages. It has been shown that these short-channel effects can be avoided by scaling down the vertical dimensions (e.g., gate insulator thickness, junction depth, etc.) along with the horizontal dimensions, while also proportionately decreasing the applied voltages and increasing the substrate doping concentration [7], [8]. Applying this scaling approach to a properly designed conventional-size MOSFET shows that a 200-Å gate insulator is required if the channel length is to be reduced to 1μ.

A major consideration of this paper is to show how the use of ion implantation leads to an improved design for very small scaled-down MOSFET's. First, the ability of ion implantation to accurately introduce a low concentration of doping atoms allows the substrate doping profile in the channel region under the gate to be increased in a controlled manner. When combined with a relatively lightly doped starting sub-

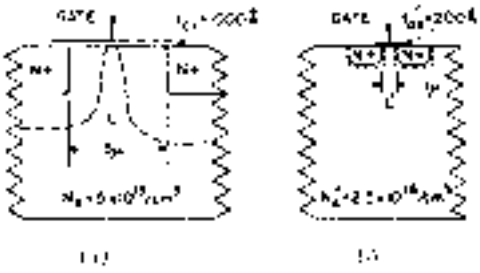

Fig. 1. Illustration of device scaling principles with κ = 5. (a) Conventional commercially available device structure. (b) Scaled-down device structure.

strate, this channel implant reduces the sensitivity of the threshold voltage to changes in the source-to-substrate ("backgate") bias. This reduced "substrate sensitivity" can then be traded off for a thicker gate insulator of 350-Å thickness which tends to be easier to fabricate reproducibly and reliably. Second, ion implantation allows the formation of very shallow source and drain regions which are more favorable with respect to short-channel effects, while maintaining an acceptable sheet resistance. The combination of these features in an all-implanted design gives a switching device which can be fabricated with a thicker gate insulator if desired, which has well-controlled threshold characteristics, and which has significantly reduced interelectrode capacitances (e.g., drain-to-gate or drain-to-substrate capacitances).

This paper begins by describing the scaling principles which are applied to a conventional MOSFET to obtain a very small device structure capable of improved performance. Experimental verification of the scaling approach is then presented. Next, the fabrication process for an improved scaled-down device structure using ion implantation is described. Design considerations for this all-implanted structure are based on two analytical tools: a simple one-dimensional model that predicts the substrate sensitivity for long channel-length devices, and a two-dimensional current-transport model that predicts the device turn-on characteristics as a function of channel length. The predicted results from both analyses are compared with experimental data. Using the two-dimensional simulation, the sensitivity of the design to various parameters is shown. Then, detailed attention is given to an alternate design, intended for zero substrate bias, which offers some advantages with respect to threshold control, Finally, the paper concludes with a discussion of the performance improvements to be expected from integrated circuits that use these very small FET's.

DEVICE SCALING

The principles of device scaling [7], [8] show in a concise manner the general design trends to be followed in decreasing the size and increasing the performance of MOSFET switching devices. Fig. 1 compares a state-of-the-art n-channel MOSFET [9] with a scaled-down device designed following the device scaling principles to be described later. The larger structure shown in Fig. 1(a) is reasonably typical of commercially available devices fabricated by using conventional diffusion techniques. It uses a 1000-Å gate insulator thickness with a substrate doping and substrate bias chosen to give a gate threshold voltage V_t of approximately 2 V relative to the source potential. A substrate doping of 5 x 10^{15} cm^{-3} is low enough to give an acceptable value of substrate sensitivity. The substrate sensitivity is an important criterion in digital switching circuits employing source followers because the design becomes difficult if the threshold voltage increases by more than a factor of two over the full range of variation of the source voltage. For the device illustrated in Fig. 1(a), the design parameters limit the channel length L to about 5μ. This restriction arises primarily from the penetration of the depletion region surrounding the drain into the area normally controlled by the gate electrode. For a maximum drain voltage of approximately 12-15 V this penetration will modify the surface potential and significantly lower the threshold voltage.

In order to design a new device suitable for smaller values of L, the device is scaled by a transformation in three variables: dimension, voltage, and doping. First, all linear dimensions are reduced by a unitless scaling factor κ, e.g. $t_{ox}' = t_{ox}/\kappa$, where the primed parameters refer to the new scaled-down device. This reduction includes vertical dimensions such as gate insulator thickness, junction depth, etc., as well as the horizontal dimensions of channel length and width. Second, the voltages applied to the device are reduced by the same factor (e.g. $V_{ds}' = V_{ds}/\kappa$). Third, the substrate doping concentration is increased, again using the same scaling factor (i.e., $N_a' = \kappa N_a$). The design shown in Fig. 1(b) was obtained using $\kappa = 5$ which corresponds to the desired reduction in channel length to 1μ.

The scaling relationships were developed by observing that the depletion layer widths in the scaled-down device are reduced in proportion to the device dimensions due to the reduced potentials and the increased doping. For example,

$$w_s' = \{[2\epsilon_{si}(\psi_b' + V_{s-sub}/\kappa)]/q\kappa N_a\}^{1/2} \simeq w_s/\kappa. \quad (1)$$

The threshold voltage at turn-on [9] is also decreased in direct proportion to the reduced device voltages so that the device will function properly in a circuit with reduced voltage levels. This is shown by the threshold voltage equation for the scaled-down device.

$$V_t' = (t_{ox}/\kappa\epsilon_{ox})\{-Q_{eff} + [2\epsilon_{Si}q\kappa N_a(\psi_s' + V_{s-sub}/\kappa)]^{1/2}\} + (\Delta W_f + \psi_s') \simeq V_t/\kappa. \quad (2)$$

In (2) the reduction in V_t is primarily due to the decreased insulator thickness, t_{ox}/κ, while the changes in the voltage and doping terms tend to cancel out. In most cases of interest (i.e., polysilicon gates of doping type opposite to that of the substrate or aluminum gates on p-type substrates) the work function difference ΔW_f is of opposite sign, and approximately cancels out ψ_s'. ψ_s' is the band bending in the silicon (i.e., the surface potential) at the onset of strong inversion for zero substrate bias. It would appear that the ψ' terms appearing in (1) and (2) prevent exact scaling since they remain approximately constant, actually increasing slightly due to the increased doping since $\psi_b' \simeq \psi_s' = (2kT/q)\ \ln(N_a'/n_i)$. However, the fixed substrate bias supply normally used with n-channel devices can be adjusted so that $(\psi_s' + V_{\text{sub}}') = (\psi_s + V_{\text{sub}})/\kappa$. Thus, by scaling down the applied substrate bias more than the other applied voltages, the potential drop across the source or drain junctions, or across the depletion region under the gate, can he reduced by κ.

All of the equations that describe the MOSFET device characteristics may be scaled as demonstrated above. For example, the MOSFET current equation [9] given by

$$I_d' = \frac{\mu_{\text{eff}}\epsilon_{\text{ox}}}{t_{\text{ox}}/\kappa}\left(\frac{W/\kappa}{L/\kappa}\right)\left(\frac{V_g - V_t - V_d/2}{\kappa}\right)\cdot (V_d/\kappa) = I_d/\kappa \qquad (3)$$

is seen to be reduced by a factor of κ, for any given set of applied voltages, assuming no change in mobility. Actually, the mobility is reduced slightly due to increased impurity scattering in the heavier doped substrate.

It is possible to generalize the scaling approach to include electric field patterns and current density. The electric field distribution is maintained in the scaled-down device except for a change in scale for the spatial coordinates. Furthermore, the electric field strength at any corresponding point is unchanged because $V/x = V'/x'$. Thus, the carrier velocity at any point is also unchanged due to scaling and, hence, any saturation velocity effects will be similar in both devices, neglecting microscopic differences due to the fixed crystal lattice dimensions. From (3), since the device current is reduced by κ, the channel current per unit of channel width W is unchanged by scaling. This is consistent with the same sheet density of carriers (i.e., electrons per unit gate area) moving at the same velocity. In the vicinity of the drain, the carriers will move away from the surface to a lesser extent in the new device, due to the shallower diffusions. Thus, the density of mobile carriers per unit volume will be higher in the space-charge region around the drain, complementing the higher density of immobile charge due to the heavier doped substrate. Other scaling relationships for power density, delay time, etc., are given in Table I and will be discussed in a subsequent section on circuit performance.

In order to verify the scaling relationships, two sets of experimental devices were fabricated with gate insulators of 1000 and 200 Å (i.e., $\kappa = 5$). The measured drain voltage characteristics of these devices, normalized to $W/L = 1$, are shown in Fig. 2. The two sets of characteristics are quite similar when plotted with voltage and current scales of the smaller device reduced by a factor of five, which confirms the scaling predictions. In Fig. 2, the exact match on the current scale is thought to be fortuitous since there is some experimental uncertainty in the magnitude of the channel length used to normalize the characteristics (see Appendix). More accurate data from devices with larger width and length dimensions on the same chip shows an approximate reduction of ten percent in mobility for devices with the heavier doped substrate. That the threshold voltage also scales correctly by a factor of five is verified in Fig. 3, which shows the experimental $\sqrt{I_d}$ versus V_g turn-on characteristics for the original and the scaled-down devices. For the cases shown, the drain voltage is large enough to cause pinchoff and the characteristics exhibit the expected linear relationship. When projected to intercept the gate voltage axis this linear relationship defines a threshold voltage useful for most logic circuit design purposes.

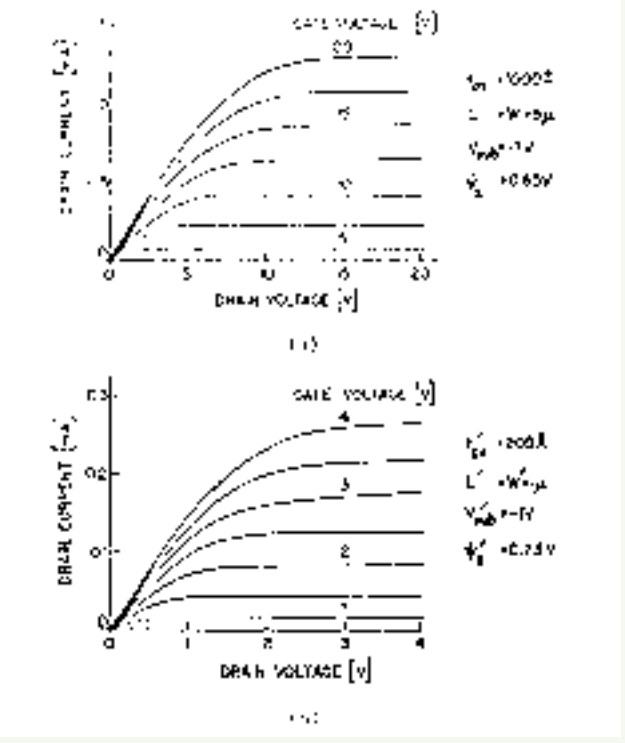

Fig. 2. Experimental drain voltage characteristics for (a) conventional, and (b) scaled-down structures shown in Fig. 1 normalized to *W/L = 1*.

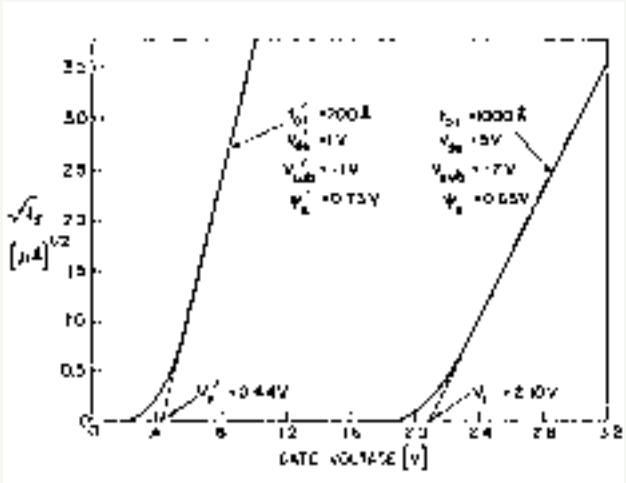

Fig. 3. Experimental turn-on characteristics for conventional and scaled-down devices shown in Fig. 1 normalized to *W/L* =1.

One area in which the device characteristics fail to scale is in the subthreshold or weak inversion region of the turn-on characteristic. Below threshold, I_d is exponentially dependent on V_g with an inverse semilogarithmic slope, α, [10], [11] which for the scaled-down device is given by

$$\alpha' \left(\frac{\text{volts}}{\text{decade}} \right) = \frac{dV_g{}'}{d \log_{10} I_d{}'} = (kT/q \log_{10} e) \left(1 + \frac{\epsilon_{Si} t_{ox}/\kappa}{\epsilon_{ox} w_d/\kappa} \right), \quad (4)$$

which is the same as for the original larger device. The parameter α is important to dynamic memory circuits because it determines the gate voltage excursion required to go from the low current "off" state to the high current "on" state [11]. In an attempt to also extend the linear scaling relationships to α one could reduce the operating temperature in (4) (i.e., $T' = T/\kappa$, but this would cause a significant increase in the effective surface mobility [12] and thereby invalidate the current scaling relationship of (3). In order to design devices for operation at room temperature and above, one must accept the fact that the subthreshold behavior does not scale as desired. This nonscaling property of the subthreshold characteristic is of particular concern to miniature dynamic memory circuits which require low source-to-drain leakage currents.

ION-IMPLANTED DEVICE DESIGN

The scaling considerations just presented lead to the device structure with a 1-μ channel length shown in Fig. 4(a). In contrast, the corresponding improved design utilizing the capability afforded by ion implantation is shown in Fig. 4(b). The ion-implanted device uses an initial substrate doping that is lower by about

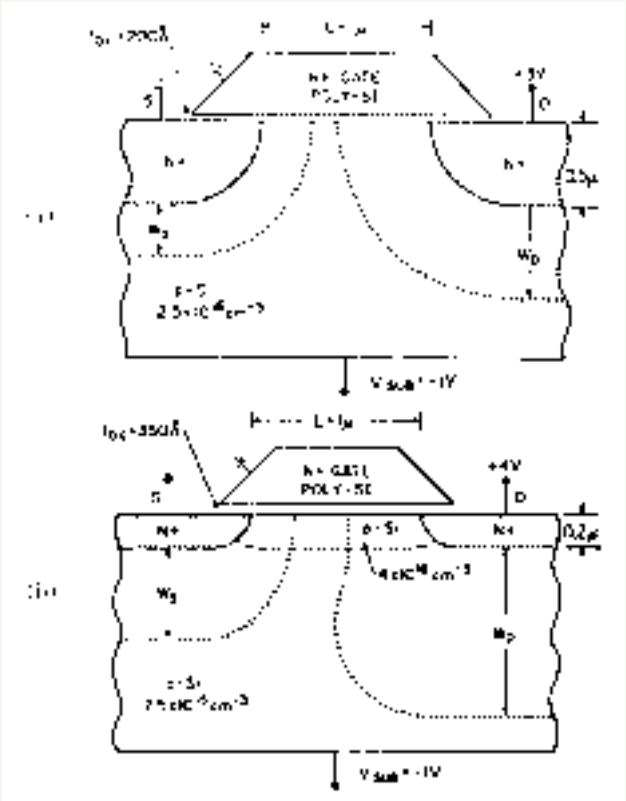

Fig. 4. Detailed cross sections for (a) scaled-down device structure, and (b) corresponding ion-implanted device structure.

a factor of four, and an implanted boron surface layer having a concentration somewhat greater than the concentration used throughout the unimplanted structure of Fig. 4(a). The concentration and the depth of the implanted surface layer are chosen so that this heavier doped region will be completely within the surface depletion layer when the device is turned on with the source grounded. Thus, when the source is biased above ground potential, the depletion layer will extend deeper into the lighter doped substrate, and the additional exposed "bulk" charge will be reasonably small and will cause only a modest increase in the gate-to-source voltage required to turn on the device. With this improvement in substrate sensitivity the gate insulator thickness can be increased to as much as 350 Å and still maintain a reasonable gate threshold voltage as will be shown later.

Another aspect of the design philosophy is to use shallow implanted n^+ regions of depth comparable to the implanted p-type surface layer. The depletion regions under the gate electrode at the edges of the source and drain are then inhibited by the heavier doped surface layer, roughly pictured in Fig. 4(b), for the case of a turned-off device. The depletion regions under the source and drain extend much further into the lighter doped substrate. With deeper junctions these depletion regions would tend to merge in the lighter doped material which would cause a loss of

threshold control or, in the extreme, punchthrough at high drain voltages. However, the shallower junctions give a more favorable electric field pattern which avoids these effects when the substrate doping concentration is properly chosen (i.e., when it is not too light).

The device capacitances are reduced with the ion-implanted structure due to the increased depletion layer width separating the source and drain from the substrate [cf. Figs. 4(a) and 4(b)], and due to the natural self-alignment afforded by the ion implantation process which reduces the overlap of the polysilicon gate over the source and drain regions. The thicker gate insulator also gives reduced gate capacitance, but the performance benefit in this respect is offset by the decreased gate field. To compensate for the thicker gate oxide and the expected threshold increase, a design objective for maximum drain voltage was set at 4 V for the ion-implanted design in Fig. 4(b), compared to 3 V for the scaled-down device of Fig.4(a).

FABRICATION OF ION-IMPLANTED MOSFET's

The fabrication process for the ion-implanted MOSFET's used in this study will now be described. A four-mask process was used to fabricate polysilicon-gate, n-channel MOSFET's on a test chip which contains devices with channel lengths ranging from 0.5 to 10 μ. Though the eventual aim is to use electron-beam pattern exposure, it was more convenient to use contact masking with high quality master masks for process development. For this purpose high resolution is required only for the gate pattern which uses lines as small as 1.5 μ which are reduced in the subsequent processing. The starting substrate resistivity was 2 Ω·cm (i.e., about 7.5×10^{15}cm^{-3}). The method of fabrication for the thick oxide isolation between adjacent FET's is not described as it is not essential to the work presented here, and because several suitable techniques are available. Following dry thermal growth of the gate oxide, low energy (40 keV), low dose (6.7×10^{11} atoms/cm^2) B^{11} ions were implanted into the wafers, raising the boron doping near the silicon surface. All implantations were performed after gate oxide growth in order to restrict diffusion of the implanted regions.

After the channel implantation, a 3500-Å thick polysilicon layer was deposited, doped n^+, and the gate regions delineated. Next, n^+ source and drain regions 2000-Å deep were formed by a high energy (100 keV), high dose (4×10^{15} atoms/cm^2) As^{75} implantation through the same 350-Å oxide layer. During this step, however, the polysilicon gate masks the channel region from the implant, absorbing all of the As^{75} dose incident there. The etching process used to delineate the gates results in a sloping sidewall which allows a slight penetration of As^{75} ions underneath the edges of the gates. The gate-to-drain (or source) overlap is estimated to be of the order of 0.2 μ. The high temperature processing steps that follow the implantations include 20 min at 900°C, and 11 min at 1000°C, which is more than adequate to anneal out the implantation damage without greatly spreading out the implanted doses. Typical sheet resistances were 50$\Omega/\square$ for the source and drain regions, and 40$\Omega/\square$ for the polysilicon areas. Following the As^{75} implant, a final insulating oxide layer 2000-Å thick was deposited using low-temperature chemical-vapor deposition. Then, the contact holes to the n^+ and polysilicon regions were defined, and the metalization was applied and delineated. Electrical contact directly to the shallow implanted source and drain regions was accomplished by a suitably chosen metallurgy to avoid junction penetration due to alloying during the final annealing step. After metalization an annealing step of 400 °C for 20 min in forming gas was performed to decrease the fast-state density.

ONE-DIMENSIONAL (LONG CHANNEL) ANALYSIS

The substrate doping profile for the 40 keV, 6.7×10^{11} atoms/cm^2 channel implant incident on the 350-Å gate oxide, is shown in Fig. 5.

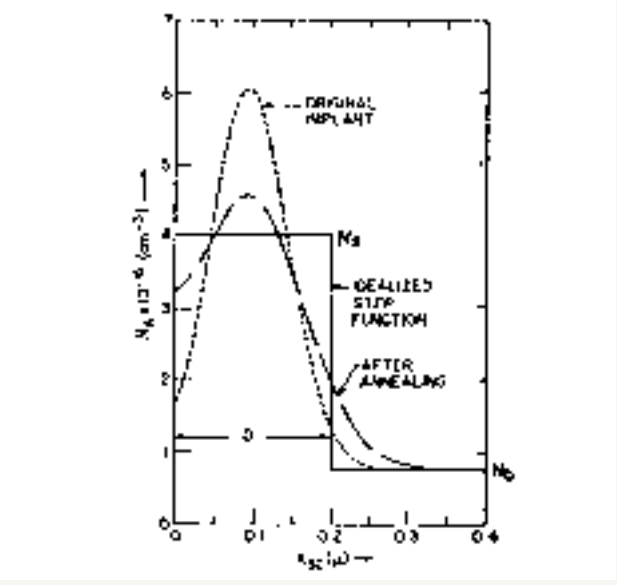

Fig. 5. Predicted substrate doping profile for basic ion-implanted device design for 40 keV B^{11} ions implanted through the 350-Å gate insulator.

Since the oxide absorbs 3 percent of the incident dose, the active dose in the silicon is 6.5×10^{11} atoms/cm^2. The concentration at the time of the implantation is given by the lightly dashed Gaussian function added to the background doping level, N_b. For 40 keV B^{11} ions, the projected range and standard deviation were taken as 1300 Å and 500 Å, respectively [13]. After the heat treatments of the subsequent

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processing, the boron is redistributed as shown by the heavier dashed line. These predicted profiles were obtained using a computer program developed by F. F. Morehead of our laboratories. The program assumes that boron atoms diffusing in the silicon reflect from the silicon-oxide interface and thereby raise the surface concentration. For modeling purposes it is convenient to use a simple, idealized, step-function representation of the doping profile, as shown by the solid line in Fig. 5. The step profile approximates the final predicted profile rather well and offers the advantage that it can be described by a few simple parameters. The three profiles shown in Fig. 5 all have the same active dose.

Using the step profile, a model for determining threshold voltage has been developed from piecewise solutions of Poisson's equation with appropriate boundary conditions [11]. The one-dimensional model considers only the vertical dimension and cannot account for horizontal short-channel effects. Results of the model are shown in Fig, 6 which plots the threshold voltage versus source-to-substrate bias for the ion-implanted step profile shown in Fig. 5. For comparison, Fig. 6 also shows the substrate sensitivity characteristics for the nonimplanted device with a 200-Å gate insulator and a constant background doping, and for a hypothetical device having a 350-Å gate insulator like the implanted structure and a constant background doping like the nonimplanted structure.

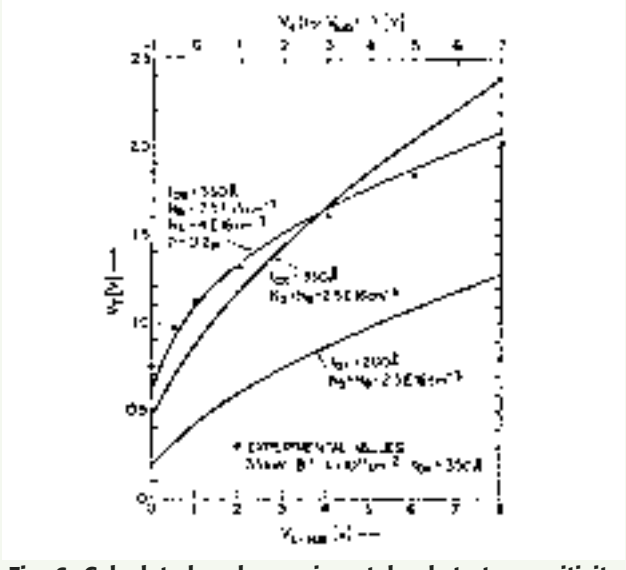

Fig. 6. Calculated and experimental substrate sensitivity characteristics for non-implanted devices with 200- and 350-Å gate insulators, and for corresponding ion-implanted device with 350-Å gate insulator.

The nonimplanted 200-Å case exhibits a low substrate sensitivity, but the magnitude of the threshold voltage is also low. On the other hand, the nonimplanted 350-Å case shows a higher threshold, but with an undesirably high substrate sensitivity. The ion-implanted case offers both a sufficiently high threshold voltage and a reasonably low substrate sensitivity, particularly for $V_{s-\text{sub}} \geq 1$ V. For $V_{s-\text{sub}} < 1$ V, a steep slope occurs because the surface inversion layer in the channel is obtained while the depletion region in the silicon under the gate does not exceed D, the step width of the heavier doped implanted region. For $V_{s-\text{sub}} \geq 1$ V, at inversion the depletion region now extends into the lighter doped substrate and the threshold voltage then increases relatively slowly with $V_{s-\text{sub}}$ [11]. Thus, with a fixed substrate bias of -1 V, the substrate sensitivity over the operating range of the source voltage (e.g., ground potential to 4 V) is reasonably low and very similar to the slope of the non- implanted 200-Å design. However, the threshold voltage is significantly higher for the implanted design which allows adequate design margin so that, under worst case conditions (e.g., short-channel effects which reduce the threshold considerably), the threshold will still be high enough so that the device can be turned off to a negligible conduction level as required for dynamic memory applications.

Experimental results are also given in Fig. 6 from measurements made on relatively long devices (i.e., $L = 10\mu$) which have no short-channel effects. These data agree reasonably well with the calculated curve. A 35 keV, 6×10^{11} atoms/cm^2 implant was used to achieve this result, rather than the slightly higher design value of 40 keV and 6.7×10^{11} atoms/cm^2.

TWO-DIMENSIONAL (SHORT CHANNEL) ANALYSIS

For devices with sufficiently short-channel lengths, the one-dimensional model is inadequate to account for the threshold voltage lowering due to penetration of the drain field into the channel region normally controlled by the gate. While some models have been developed which account for this behavior [14], the problem is complicated for the ion-implanted structure by the non-uniform doping profile which leads to an electric field pattern that is difficult to approximate. For the ion-implanted case, the two-dimensional numerical current transport model of Kennedy and Mock [15], [16] was utilized. The computer program was modified by W. Chang and P. Hwang [17] to handle the abrupt substrate doping profiles considered for these devices.

The numerical current transport model was used to calculate the turn-on behavior of the ion-implanted device by a point-by-point computation of the device current for increasing values of gate voltage. Calculated results are shown in Fig. 7 for two values of channel length in the range of 1μ, as well as for a relatively long-channel device with $L = 10\mu$. All cases were normalized to a width-to-length ratio of unity, and a drain voltage of 4 V was used in all cases. As the channel length

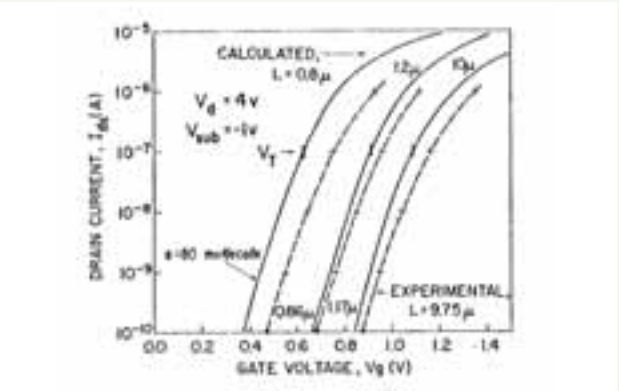

Fig. 7. Calculated and experimental subthreshold turn-on characteristic for basic ion-implanted design for various channel lengths with V_{sub} = -1V, V_d = 4V.

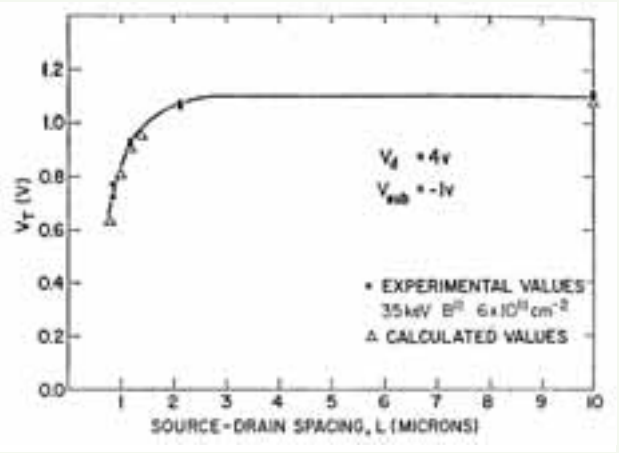

Fig. 8. Experimental and calculated dependence of threshold voltage on channel length for basic ion-implanted design with V_{sub}=-1V, V_d = 4V.

is reduced to the order of 1μ, the turn-on characteristic shifts to a lower gate voltage due to a lowering of the threshold voltage. The threshold voltage occurs at about 10^{-7} A where the turn-on characteristics make a transition from the exponential subthreshold behavior (a linear response on this semilogarithmic plot) to the $I_d \propto V_g{}^2$ square-law behavior. This current level can also be identified from Fig. 3 as the actual current at the projected threshold voltage, V_t. When the computed characteristics were plotted in the manner of Fig. 3 they gave 4×10^{-8} A at threshold for all device lengths. The band bending, ψ_s, at this threshold condition is approximately 0.75 V. Some of the other device designs considered with heavier substrate concentrations gave a higher current at threshold, so, for simplicity, the value of 10^{-7} A was used in all cases with a resultant small error in V_t.

MOSFET's with various channel lengths were measured to test the predictions of the two-dimensional model. The technique for experimentally determining the channel length for very short devices is described in the Appendix. The experimental results are plotted in Fig. 7 and show good agreement with the calculated curves, especially considering the somewhat different values of L. Another form of presentation of this data is shown in Fig. 8 where the threshold voltage is plotted as a function of channel length. The threshold voltage is essentially constant for $L > 2\mu$, and falls by a reasonably small amount as L is decreased from 2 to 1 μ, and then decreases more rapidly with further reductions in L. For circuit applications the nominal value of L could be set somewhat greater than 1 μ so that, over an expected range of deviation of L, the threshold voltage is reasonably well controlled.

For example, $L = 1.3\pm0.3\mu$ would give $V_t = 1.0\pm0.1$ V from chip to chip due to this short-channel effect alone. This would be tolerable for many circuit applications because of the tracking of different devices on a given chip, if indeed this degree of control of L can be achieved. The experimental drain characteristics for an ion-implanted MOSFET with a 1.1-μ channel length are shown in Fig. 9 for the grounded source condition. The gener-

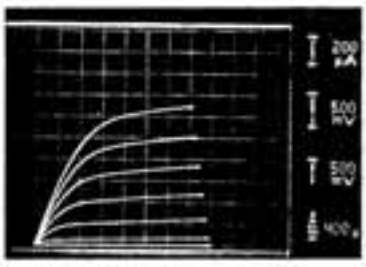

Fig. 9. Experimental drain voltage characteristics for basic ion-implanted design with V_{sub} = 1V, L = 1.1μ, and w = 12.2μ. Curve tracer parameters; load resistance 30Ω, drain voltage 4 V, gate voltage 0-4V in 8 steps each 0.5 V apart.

al shape of the characteristics is the same as those observed for much larger devices. No extraneous short-channel effects were observed for drain voltages as large as 4 V. The experimental data in Figs. 6 - 9 were taken from devices using a B^{11} channel implantation energy and dose of 35 keV and 6.0×10^{11} atoms/cm^2, respectively.

The two-dimensional simulations were also used to test the sensitivity of the design to various parameters. The results are given in Fig. 10, which tabulates values of threshold voltage as a function of channel length for the indicated voltages. Fig. 10(a) is an idealized representation for the basic design that has been discussed thus far. The first perturbation to the basic design was an increase in junction depth to 0.4 μ. This was found to give an appreciable reduction in threshold voltage for the shorter devices in Fig. 10(b). Viewed another way, the minimum device length would have to be increased by 20 percent (from 1.0 to 1.2 μ) to obtain a threshold comparable

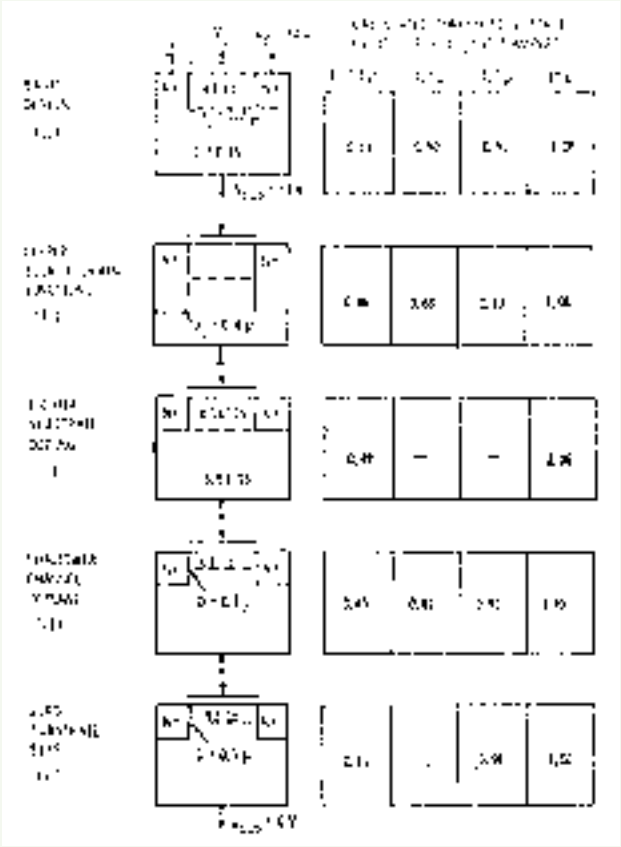

Fig. 10. Threshold voltage calculated using two-dimensional current transport model for various parameter conditions. A flat-band voltage of -1.1 V is assumed.

to the basic design. This puts the value of the shallower junctions in perspective. Another perturbation from the basic design which was considered was the use of a substrate doping lighter by a factor of 2, with a slightly higher concentration in the surface layer to give the same threshold for a long-channel device [Fig. 10(c)]. The results for smaller devices proved to be similar to the case of deeper junctions. The next possible departure from the basic design is the use of a shallower boron implantation in the channel region, only half as deep, with a heavier concentration to give the same long-channel threshold [Fig. 10(d)]. With the shallower profile, and considering that the boron dose implanted in the silicon is about 20 percent less in this case, it was expected that more short-channel effects would occur. However, the calculated values show almost identical thresholds compared to the basic design. With the shallower implantation it is possible to use zero substrate bias and still have good substrate sensitivity since the heavier doped region is completely depleted at turn-on with a grounded source. The last design perturbation considers such a case, again with a heavier concentration to give the same long-channel threshold [Fig. 10 (e)]. The calculations for this case show appreciably less short-channel effect. In fact, the threshold for this case for a device with $L = 0.8\mu$ is about the same as for an $L = 1.0\mu$ device of the basic design. This important improvement is apparently due to the reduced depletion layer widths around the source and drain with the lower voltage drop across those junctions. Also, with these bias and doping conditions, the depletion layer depth in the silicon under the gate is much less at threshold, particularly near the source where only the band bending, ψ_s, appears across this depletion region, which may help prevent the penetration of field lines from the drain into this region where the device turn-on is controlled.

CHARACTERISTICS OF THE ZERO SUBSTRATE BIAS DESIGN

Since the last design shown in Fig. 10(e) appears to be better behaved in terms of short-channel effects, it is worthwhile to review its properties more fully. Experimental devices corresponding to this design were built and tested with various channel lengths. In this case a 20 ke V, 6.0×10^{11} atoms/cm^2 B^{11} implant was used to obtain a shallower implanted layer of approximately 1000-Å depth [11]. Data on threshold voltage for these devices with 4 V applied to the drain is presented in Fig. 11 and corresponds very well to the calculated values. Data for a small drain voltage is also given in this figure, showing much less variation of threshold with channel length, as expected. The dependence of threshold voltage on source-to-substrate bias is shown in Fig. 12 for different values of L. The drain-to-source voltage was held at a constant low value for this measurement. The results show that the substrate sensitivity is indeed about the same for this design with zero substrate bias as for the original design with $V_{sub} = -1$ V. Note that the smaller devices show a somewhat flatter substrate sensitivity characteristic with relatively lower thresholds at high values of source (and drain) voltage.

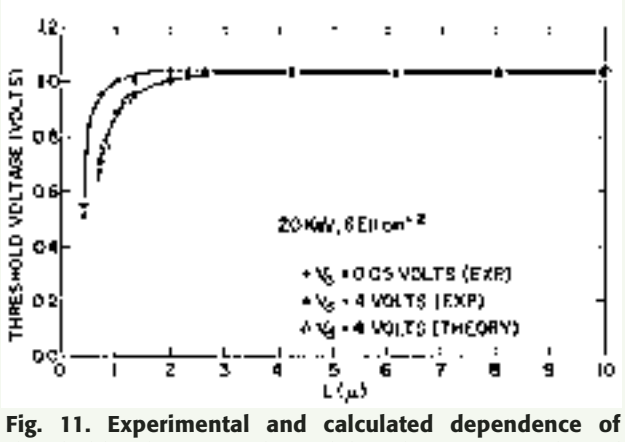

Fig. 11. Experimental and calculated dependence of threshold voltage on channel length for ion-implanted zero substrate bias design.

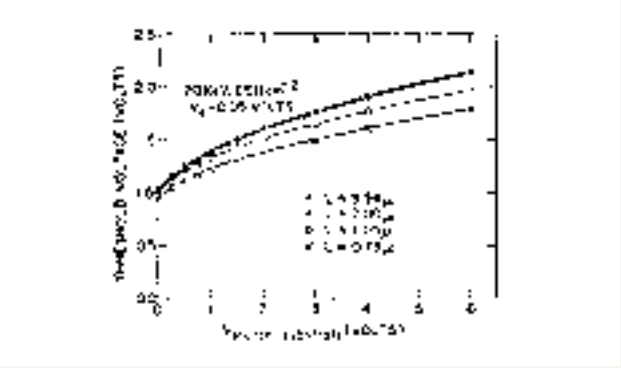

Fig. 12. Substrate sensitivity characteristics for ion-implanted zero substrate bias design with channel length as parameter.

The turn-on characteristics for the zero substrate bias design, both experimental and calculated, are shown in Fig. 13 for different values of L. The relatively small shift in threshold for the short-channel devices is evident; however, the turn-on rate is considerably slower for this case than for the $V_{sub} = -1$ V case shown in Fig. 7. This is due to the fact that the depletion region in the silicon under the gate is very shallow for this zero substrate bias case so that a large portion of a given gate voltage change is dropped across the gate insulator capacitance rather than across the silicon depletion layer capacitance. This is discussed in some detail for these devices in another paper [11]. The consequence for dynamic memory applications is that, even though the zero substrate bias design offers improved threshold control for strong inversion, this advantage is offset by the flatter subthreshold turn-on characteristic. For such applications the noise margin with the turn-on characteristic of Fig. 13 is barely suitable if the device is turned off by bringing its gate to ground. Furthermore, elevated temperature aggravates the situation [18]. Thus, for dynamic memory, the basic design with $V_{sub} = -1$ V presented earlier is preferred.

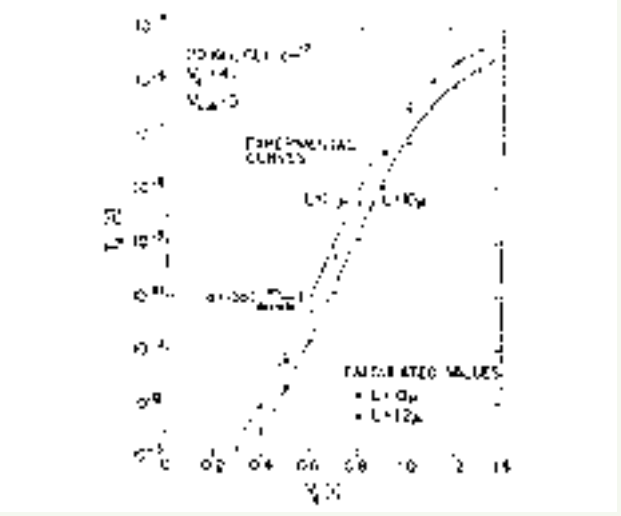

Fig. 13. Calculated and experimental subthreshold turn-on characteristics for ion-implanted zero substrate bias design.

CIRCUIT PERFORMANCE WITH SCALED-DOWN DEVICES

The performance improvement expected from using very small MOSFET's in integrated circuits of comparably small dimensions is discussed in this section. First, the performance changes due to size reduction alone are obtained from the scaling considerations given earlier. The influence on the circuit performance due to the structural changes of the ion-implanted design is then discussed.

Table I lists the changes in integrated circuit performance which follow from scaling the circuit dimensions, voltages, and substrate doping in the same manner as the device changes described with respect to Fig. 1. These changes are indicated in terms of the dimensionless scaling factor κ.

TABLE I
SCALING RESULTS FOR CIRCUIT PERFORMANCE

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time per circuit VC/I	$1/\kappa$
Power dissipation per circuit VI	$1/\kappa^2$
Power density VI/A	1

Justifying these results here in great detail would be tedious, so only a simplified treatment is given. It is argued that all nodal voltages are reduced in the miniaturized circuits in proportion to the reduced supply voltages. This follows because the quiescent voltage levels in digital MOSFET circuits are either the supply levels or some intermediate level given by a voltage divider consisting of two or more devices, and because the resistance V/I of each device is unchanged by scaling. An assumption is made that parasitic resistance elements are either negligible or unchanged by scaling, which will be examined subsequently. The circuits operate properly at lower voltages because the device threshold voltage V_t scales as shown in (2), and furthermore because the tolerance spreads on V_t should be proportionately reduced as well if each parameter in (2) is controlled to the same percentage accuracy. Noise margins are reduced, but at the same time internally generated noise coupling voltages are reduced by the lower signal voltage swings.

Due to the reduction in dimensions, all circuit elements (i.e., interconnection lines as well as devices)

will have their capacitances reduced by a factor of κ. This occurs because of the reduction by κ^2 in the area of these components, which is partially cancelled by the decrease in the electrode spacing by κ due to thinner insulating films and reduced depletion layer widths. These reduced capacitances are driven by the unchanged device resistances V/I giving decreased transition times with a resultant reduction in the delay time of each circuit by a factor of κ. The power dissipation of each circuit is reduced by κ^2 due to the reduced voltage and current levels, so the power-delay product is improved by κ^3. Since the area of a given device or circuit is also reduced by κ^2, the power density remains constant. Thus, even if many more circuits are placed on a given integrated circuit chip, the cooling problem is essentially unchanged.

TABLE II
SCALING RESULTS FOR INTERCONNECTION LINES

Parameter	Scaling Factor
Line resistance, $R_L = \rho L/Wt$	κ
Normalized voltage drop IR_L/V	κ
Line response time R_LC	1
Line current density I/A	κ

As indicated in Table II, a number of problems arise from the fact that the cross-sectional area of conductors is decreased by κ^2 while the length is decreased only by κ. It is assumed here that the thicknesses of the conductors are necessarily reduced along with the widths because of the more stringent resolution requirements (e.g., on etching, etc.). The conductivity is considered to remain constant which is reasonable for metal films down to very small dimensions (until the mean free path becomes comparable to the thickness), and is also reasonable for degenerately doped semiconducting lines where solid solubility and impurity scattering considerations limit any increase in conductivity. Under these assumptions the resistance of a given line increases directly with the scaling factor κ. The IR drop in such a line is therefore constant (with the decreased current levels), but is κ times greater in comparison to the lower operating voltages. The response time of an unterminated transmission line is characteristically limited by its time constant R_LC, which is unchanged by scaling; however, this makes it difficult to take advantage of the higher switching speeds inherent in the scaled-down devices when signal propagation over long lines is involved. Also, the current density in a scaled-down conductor is increased by κ, which causes a reliability concern. In conventional MOSFET circuits, these conductivity problems are relatively minor, but they become significant for linewidths of micron dimensions. The problems may he circumvented in high performance circuits by widening the power buses and by avoiding the use of n^+ doped lines for signal propagation.

Use of the ion-implanted devices considered in this paper will give similar performance improvement to that of the scaled-down device with $\kappa = 5$ given in Table I. For the implanted devices with the higher operating voltages (4 V instead of 3 V) and higher threshold voltages (0.9 V instead of 0.4 V), the current level will be reduced in proportion to $(V_g - V_t)^2/t_{ox}$ to about 80 percent of the current in the scaled-down device. The power dissipation per circuit is thus about the same in both cases. All device capacitances are about a factor of two less in the implanted devices, and n^+ interconnection lines will show the same improvement due to the lighter substrate doping and decreased junction depth. Some capacitance elements such as metal interconnection lines would be essentially unchanged so that the overall capacitance improvement in a typical circuit would be somewhat less than a factor of two. The delay time per circuit which is proportional to VC/I thus appears to be about the same for the implanted and for the directly scaled-down micron devices shown in Fig. 4.

SUMMARY

This paper has considered the design, fabrication, and characterization of very small MOSFET switching devices. These considerations are applicable to highly miniaturized integrated circuits fabricated by high-resolution lithographic techniques such as electron-beam pattern writing. A consistent set of scaling relationships were presented that show how a conventional device can be reduced in size; however, this direct scaling approach leads to some challenging technological requirements such as very thin gate insulators. It was then shown how an all ion-implanted structure can be used to overcome these difficulties without sacrificing device area or performance. A two-dimensional current transport model modified for use with ion-implanted structures proved particularly valuable in predicting the relative degree of short-channel effects arising from different device parameter combinations. The general objective of the study was to design an n-channel polysilicon-gate MOSFET with a 1-μ channel length for high-density source-follower circuits such as those used in dynamic memories. The most satisfactory combination of subthreshold turn-on range, threshold control, and substrate sensitivity was achieved by an experimental MOSFET that used a 35 keV, 6.0×10^{11} atoms/cm^2 B^{11} channel implant, a 100 keV, 4×10^{15} atoms/cm^2 As^{75} source/drain implant, a 350-Å gate insulator, and an applied substrate bias of –1 V. Also presented was an ion-implanted design intended for zero substrate bias that is more attractive from the point of view of

threshold control but suffers from an increased subthreshold turn-on range. Finally the sizable performance improvement expected from using very small MOSFET's in integrated circuits of comparably small dimensions was projected.

APPENDIX
EXPERIMENTAL DETERMINATION OF CHANNEL LENGTH

A technique for determining the effective electrical channel length L for very small MOSFET's from experimental data is described here. The technique is based on the observation that

$$W R_{\text{chan}} = L \rho_{\text{chan}} \qquad (A1)$$

where R_{chan} is the channel resistance, and ρ_{chan} the sheet resistance of the channel. For a fixed value of $V_g - V_t > 0$, and with the device turned on in the below-pinchoff region, the channel sheet resistance is relatively independent of L. Then, a plot of $W R_{\text{chan}}$ versus L_{mask} will intercept the L_{mask} axis at ΔL because $\Delta L = L_{\text{mask}} - L$, where ΔL is the processing reduction in the mask dimension due to exposure and etching. An example of this technique is illustrated in Fig. 14.

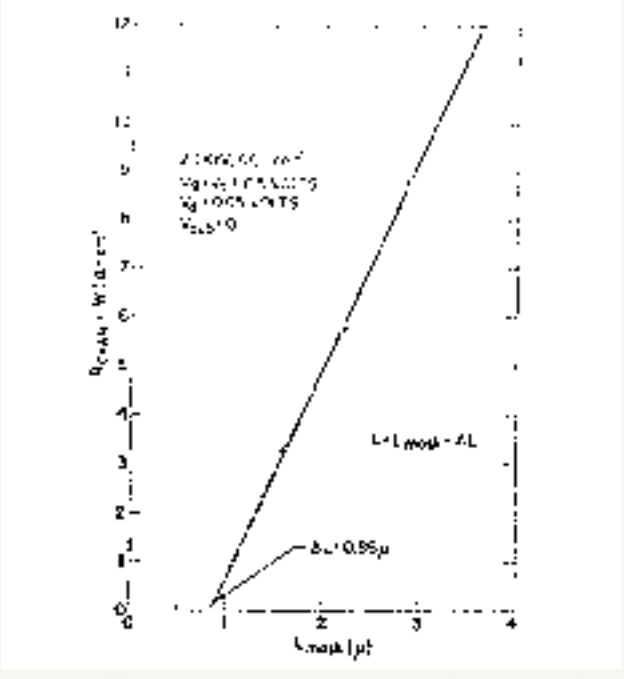

Fig. 14. Illustration of experimental technique used to determine channel length, L.

The experimental values of W and R_{chan} used in Fig. 14 were obtained as follows. First, the sheet resistance of the ion-implanted n^+ region was determined using a relatively large four-point probe structure. Knowing the n^+ sheet resistance allows us to compute the source and drain resistance R_s and R_d, and to deduce W from the resistance of a long, slender, n^+ line. The channel resistance can be calculated from

$$R_{\text{chan}} = V_{\text{chan}}/I_d = (V_d - I_d(R_s + R_d + 2R_c + R_{\text{load}}))/I_d, \quad (A2)$$

where R_c is the contact resistance of the source or drain, and R_{load} is the load resistance of the measurement circuit. I_d was determined at $V_g = V_t + 0.5$ V with a small applied drain voltage of 50 or 100 mV. The procedure is more simple and accurate if one uses a set of MOSFET's having different values of L_{mask} but all with the same value of W_{mask}. Then one needs only to plot R_{chan} versus L_{mask} in order to determine ΔL.

Acknowledgements

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Prior to 1966 he served as Assistant Professor in the Department of Electrical Engineering, Technical University of Munich, Munich, Germany. During this period he was working on the synthesis of linear and digital networks. In 1966 he joined the IBM T. J. Watson Research Center, Yorktown Heights, N.Y., where he is currently a member of a semiconductor device and process design group. His current technical interests involve various aspects of advanced integrated circuits like miniaturization, device simulation, and ion implantation. From September 1973 he was on a one year assignment at the IBM Laboratory, Boeblingen, Germany.

Dr. Gaensslen is a member of the Nachrichtentechnische Gesellschaft.

Hwa-Nien Yu (M'65) was born in Shanghai, China, on January 17, 1929. He received the B.S., MS., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana, in 1953, 1954, and 1958, respectively. While at the University, he was a Research Assistant in the Digital Computer Laboratory and worked on the design of the Illiac-II computer. Since joining the IBM Research Laboratory in 1957, he has been engaged in various exploratory solid-state device research activities. After working with the Advanced Systems Development Division from 1959 to 1962, he rejoined the Research Division in 1962 to work on the ultra-high speed germanium device technology. Since 1967, he has been engaged in advanced silicon LSI device technology research. He is currently the Manager of Semiconductor Technology at the IBM T. J. Watson Research Center, Yorktown Heights, N.Y.

Dr. Yu is a member of Sigma Xi.

V. Leo Rideout (S'61—M'65) was born in N.J. in 1941. He received the BS.E.E. degree with honors in 1963 from the University of Wisconsin, Madison, the

M,S.E.E. degree in 1964 from Stanford University, Stanford, Calif., and the Ph.D. degree in materials science in 1970 from the University of Southern California (U.S.C.), Los Angeles. His thesis work at U.S.C. under Prof. C. H. Crowell concerned thermally assisted current transport in platinum silicide Schottky barriers.

From 1963 to 1965 he was a member of the technical staff of Bell Telephone Laboratories where he worked on high-frequency germanium transistors and metal-semiconductor Schottky barriers on potassium tantalate. In 1966 he spent a year as a Research Assistant in the department of Materials Science at the Technological University of Eindhoven, Eindhoven, The Netherlands, studying acoustoelectric effects in cadmium sulphide. In 1970 he joined IBM Research in the device research group of Dr. L. Esaki where he worked on fabrication and contact technology for multiheterojunction "superlattice" structures using gallium-arsenide-phosphide and gallium-aluminum-arsenide. Since 1972 he has been a member of the semiconductor device and circuit design group of Dr. R. Dennard at the IBM T. J. Watson Research Center, Yorktown Heights, N.Y. His present research interests concern high density silicon FET technology. He is the author or co-author of 20 technical papers and 3 US. Patents.

Dr. Rideout is a member of the Electrochemical Society, Tau Beta Pi, Eta Kappa Nu, Phi Kappa Phi, and Sigma Xi.

Ernest Bassous was born in Alexandria, Egypt, on September 1, 1931. He received the B.Sc. degree in chemistry from the University of London, London, England in 1953, and the M.S. degree in physical chemistry from the Polytechnic Institute of Brooklyn, Brooklyn, N.Y. in 1965.

From 1954 to 1959 he taught Chemistry and Physics at the British Boys' School, Alexandria, Egypt. He went to France in 1959 where he worked for one year on infra red detectors at the Centre National d'Etudes des Telecommunications, Issy-les-Moulineaux, Seine. From 1960 to 1964 he worked at the Thomas A. Edison Research Laboratory in West Orange, N.J., where his activities included studies in arc discharge phenomena, ultra violet absorption spectroscopy, and organic semiconductors. In 1964 he joined the IBM Research Laboratory, Yorktown Heights, N.Y., to work on semiconductors. As a member of the Research staff he is presently engaged in the study of materials and processes used in the fabrication of silicon integrated circuits.

Mr. Bassous is a member of the Electrochemical Society and the American Association for the Advancement of Science.

Andre R. LeBlanc (M'74) received the B.S. degree in electrical engineering, and the M.S. degree in physics from the University of Vermont, Burlington, in 1956 and 1959, respectively, and the D.Sc. degree in electrical engineering from the University of New Mexico, Albuquerque, in 1962.

Prior to joining IBM, Essex Junction, Vt., in 1957, he was affiliated with G.E. as an electrical engineer and also with Sandia Corporation in conjunction with the University of New Mexico. In 1959 he took an educational leave of absence to complete his doctorate. He is presently a member of the Exploratory Memory Group at the IBM Laboratory, Essex Junction, where his current technical interest includes a study of short-channel MOSFET devices. He has authored five publications and twelve papers, as well as several IBM Technical Reports.

Dr. LeBlanc is a member of Sigma Xi and Tau Beta Pi.

An Interview with James Meindl 2006 IEEE Medal of Honor Receipient

Microelectronics pioneer recognized with highest IEEE award

James Meindl, friend and pioneer of the solid-state circuits community was recognized in 2006 with the highest IEEE award, the IEEE Medal of Honor, "for pioneering contributions to microelectronics, including low power, biomedical, physical limits and on-chip interconnect networks." Meindl, a prolific author, energetic mentor and broad thinker, accepted the award as the highlight of the IEEE Honors ceremony in June 2006.

Besides his outstanding technical contributions, Meindl is well known to the solid-state circuits community for his service in many important roles, serving as the first editor of the JSSC and chair of the ISSCC. In 2003 ISSCC recognized Meindl as the author with the highest number of ISSCC papers during its first 50 years. He has more than 360 authored papers in IEEEXplore.

James Meindl receiving the IEEE Medal of Honor June 2006 at the IEEE award ceremony.

Q and A

Meindl the Mentor

Publishing 360 papers requires a lot of human interconnection, with students and co-authors. Meindl is an important force in generating productive graduate students and industry leaders. Over his career, he has supervised over 80 Ph.D. graduates at Stanford University, Rensselaer Polytechnic Institute and Georgia Institute of Technology, many of whom have gone on to have profound impact on the semiconductor industry.

Q. How do you select your graduate students?

A. The prime qualities I look for in selecting graduate students are ability/talent, motivation/commitment, interpersonal skill/friendliness, integrity and responsiveness. The best test for these qualities is to engage the student in a one quarter/semester special projects course prior to any decision regarding a Ph.D. commitment. For overseas students, this is often not feasible and then at least a one academic year commitment with support is necessary based on a resume and phone calls.

Q. What about written versus oral qualifying exams?

A. Even though it was new to me when I started on the faculty at Stanford, I learned to prefer the oral over a written exam because the personal interaction with the student under challenging conditions is extremely revealing. Observing the student "thinking out loud and responding to clues" is most informative.

Q. On picking thesis topics?

A. My favorite word of advice to a Ph.D. student is "try the simplest case," which I learned from Professor William Shockley, Nobel Prize Recipient for the invention of the transistor, whose office was only two doors away from me at Stanford.

Q. How successful have you been predicting your students' accomplishments?

A. I have had my share of surprises not as often related to thesis research productivity as to down stream professional accomplishments that I might have (or not have) projected. Higher level professional accomplishments are strongly related to "people skills." My favorite question for myself regarding a Ph.D. graduate is "what did he do best?"

Researching the Future

Q. Defining problems, researching to find solutions, communicating the solutions, presenting and writing which of these is most fun and which is hardest?

A. The most fun is finding an elegant new solution and this is what I strive to encourage every student to experience. Nothing is more challenging than asking the right question in unambiguous terms at the right time. Checking solutions and interpreting them to extract deep insights are important aspects of Ph.D. research that I learned well at Carnegie Tech in the 1950's.

Q. What are the pros and cons of research that ends up in the public domain versus the research destined for privately held and licensed patents?

A. The IP issues of today are complex and can be vexing. The SRC/MARCO Focus Center Program, supported by a consortium of US companies and DARPA, has what I have found to be a quite reasonable

approach to IP ownership: MARCO receives a non-exclusive royalty-free license to all foreground IP and reasonable assurance that any critical background IP will be licensed for a reasonable royalty. Giving more authority to the Provost's office to negotiate IP agreements should help the current situation. To be competitive globally, US companies now need university research results and the best interests of the country are served when this happens.

Q. What are the new hot areas that for the next decade?

A. Electronics and more specifically ICs have been the principal driver of the most important economic event of the past half century, the information revolution. My view of the critical reason for the unprecedented impact of the IC is that it represents a fusion of the top-down and bottom-up approaches to microelectronics that has now evolved to become nanoelectronics. Scaling is our common term for the top-down approach. The bottom-up approach is epitomized by the self-assembled single crystal silicon ingot from which (now 300mm) silicon wafers are sliced, each yielding several hundred chips each now containing several billion transistors.

Of course Moore's Law will cease, perhaps in a 10-20 year timeframe. But my crystal ball suggests IC manufacturing will be important for more than double that number of years. The "vacuum tube-to-transistor like" breakthrough that is needed to replace ICs will require a much more elegant and still unknown fusion of top-down nanotechnology in the sub-10nm range with self-assembled bottom-up nanotechnology probably rooted in biochemical science.

Meindl accepted his award with these comments about technology.

Early 21st century microchips are a marvelous consequence of a "fusion of the top-down and bottom-up approaches to nanotechnololgy." Top-down nanotechnology has been used to pattern and produce multibillion transistor chips with minimum feature sizes now beyond 50 nm. Bottom-up nanotechnology has been used to produce self-assembled single crystal ingots of silicon that are sliced to provide 300 mm diameter wafers for microchip manufacturing. One broad prospective is that to advance beyond the ultimate limits of CMOS integrated electronics will require an elegant fusion of top-down and bottom-up nanotechnology enabled by future discoveries and inventions in both physical and biological science and engineering as profound as the mid-20th century inventions of the transistor and the integrated circuit. Carbon nanotube and graphene nanoribbon technologies represent primitive examples of efforts to achieve such a fusion.

The first Editor, James Meindl, then of the US Army Electronics Command had to be very diligent in his search for both adequate quantity and quality of papers for his first issues.

From the beginning, a decision was made that a major source of papers for the JSSC should be the full-length versions of papers first presented at the ISSCC. However, this aspect took time. Many of the conference speakers at the ISSCC were not accustomed to publishing in refereed scholarly publications. After the vigorous refereeing and selection process for paper presentation at the ISSCC, it was necessary to work rather carefully with prospective authors to encourage them for further effort to achieve the results for adequate publication in a major journal of the IEEE.

Dr. Meindl, as the first Editor made significant contributions, not only in working with the authors to publish their good contributions in spite of the press of their dealing on a daily basis with the exploding technology of solid-state circuits and devices. In addition he set the tone for the Journal of Solid-State Circuits. In short order he was able to achieve a high standard of quality and was able to establish a pattern of publishing major ISSCC presentations as regular title papers…

From "The Origin of the Journal, the Council and the Conference of Solid-State Circuits" by Donald O. Pederson, JSSC, April 1984

About James Meindl

Early in his career, Dr. Meindl developed micropower integrated circuits for portable military equipment at the U.S. Army Electronics Laboratory in Fort Monmouth, New Jersey. He then joined Stanford University in Palo Alto, California, where he developed low-power integrated circuits and sensors for a portable electronic reading aid for the blind, miniature wireless radio telemetry systems for biomedical research, and non-invasive ultrasonic imaging and blood-flow measurement systems. Dr. Meindl was the founding director of the Integrated Circuits Laboratory and a founding co-director of the Center for Integrated Systems at Stanford. The latter was a model for university and industry cooperative research in microelectronics.

From 1986 to 1993, Dr. Meindl was senior vice president for academic affairs and provost of Rensselaer Polytechnic Institute in Troy, New York. In this role he was responsible for all teaching and research.

He joined Georgia Tech in 1993 as director of its Microelectronic Research Center. In 1998, he became the founding director of the Interconnect Focus Center, where he led a team of more than

60 faculty members from MIT, Stanford, Rensselaer, SUNY Albany, and Georgia Tech in a partnership with industry and government. His research at Georgia Tech includes exploring different solutions for solving interconnectivity problems that arise from trying to interconnect billions of transistors within a tiny chip.

An IEEE Life Fellow, Dr. Meindl is the recipient of the Benjamin Garver Lamme Medal of the American Association for Engineering Education, the J.J.Ebers Award of the IEEE Electron Devices Society, the IEEE Education Medal and the IEEE Solid State Circuits Award.

Hugo De Man Awarded for Leadership in Integrated Circuit Design and Design Methodology

Founder of IMEC recognized with highest SSCS award

Hugo De Man, Professor Emeritus at the Katholieke Universitiet, Leuven, Belgium, is the recipient of the 2007 IEEE Donald O. Pederson Technical Field Award in Solid-State Circuits.

Hugo De Man, Professor Emeritus at the Katholieke Universiteit, Leuven, Belgium will receive the IEEE Donald O. Pederson Technical Field Award in Solid-State Circuits, on Monday 12 February 2007 at the ISSCC for leadership in integrated circuit design and design methodology.

Jan Rabaey, a U.C. Berkeley professor and a former graduate student of De Man notes that De Man is responsible for "many firsts in the computer-aided design world - mixed-mode simulation, switched-capacitor simulation, digital signal processing optimization, high-level synthesis for DSP, silicon compilation, system-level design. De Man was also the first to use the term and ideas of 'Meet-in-the-middle design methodology', which is the basis of the platform based design methodology (this in the early 1980s!) And De Man has major impacts on digital design" and Rabaey cites the NORA CMOS as an example. NORA stands for "No Race," which has precharge and evaluation properties that enable one to design simple testing circuits for output stuck-at-zero, stuck-at-one, stuck-open and stuck-on faults.

Georges Gielen, professor at K. U. Leuven, lists fields that De Man has contributed to: "advanced simulation (switched capacitors), high-level synthesis (the different Cathedral projects), hardware-software co-design, etc." Much of this work has been taken up by spin-offs such as Silvar Lisco, EDC, and CoWare. "His contributions to the development of innovative design methodologies and related EDA tools have enabled the design of multi-million-transistor chips. Hugo and his colleagues have built IMEC (the Inter-University Microelectronics Center) and K.U. Leuven into the pre-eminent microelectronics research center in Europe."

Rabaey recalls from their joint projects that De Man "was quick to observe that simulation techniques used for mixed-mode simulation as developed in the DIANA program could be easily adopted to analyze discrete-time analog systems as well. This was the beginning of the development of a sophisticated environment that ultimately covered all aspects of switched-capacitor design, and was commercialized by Silvar-Lisco. A second project where I collaborated with him was on the now 'infamous' Cathedral projects, which really brought high-level synthesis to the foreground. Again, Hugo observed early on that digital signal processing was an area where design automation could have a big impact. Cathedral was widely known as one of the first (and maybe last) instances of high-level synthesis that was adopted in industry."

His Royal Highness, the late King of Belgium, Boudewijn, talking with Hugo De Man while visiting the microelectronics lab at the University of Leuven in the seventies.

The IMEC Challenge

De Man comments that joining Roger Van Overstraeten's team in 1983 to set up IMEC was the greatest challenge of his career. IMEC is an independent research institute covering all aspects of micro-elec-

tronics and combining international contract research by top players in the field with doctoral level research, teaching and publications. According to Cor Claeys, a current Research Head at IMEC, it was formed from a small research group of about 20 people at the University of Leuven. By the beginning of this decade IMEC had became the largest such group in Europe with 125 professional researchers. Dave Hodges who knew and worked with him during De Man's time as a post-doc at U.C. Berkeley, 1970-71, says that De Man and others "built IMEC into the pre-eminent microelectronics research center in Europe. It was always clear that he is a man with many talents. He and his students have contributed much to the progress of microelectronics."

De Man explains, "IMEC helped in creating a great mixed industry-university team to build a successful research program on DSP silicon compilation, the results of which are still in use today. And most of the team members have either created their own spin-off companies, are captains of industry or top level academics. So the greatest challenge became also the greatest fun as there is no satisfaction without overcoming some challenge first."

Willy Sansen, Head of ESAT-MICAS at K.U. Leuven, reports that De Man's "task has been to look around and provide advice to the policymakers of IMEC. He does this exceedingly well!"

De Man Looks Back

"I was extremely lucky to meet two extra-ordinary visionary mentors who both became friends for life: Roger Van Overstraeten and Don Pederson. The first opened the world of physics and technology for me, the second introduced me to the passion of circuit and system design and so many other good things in life.

Common to both was the vision that you never walk alone but that great things only happen when you stimulate the best people to join forces and have fun in doing so. For that reason receiving the Don Pederson award is so dear to me as I owe a lot to him, as does everyone who had the privilege to work with him.

Another factor of luck is that I belong to a generation that could participate in the 60-year evolution from the single transistor circuit to the billion-transistor chip. Perhaps one of the most fascinating periods in engineering history, although you never know."

Inspired Educator

De Man's lectures were by far the most inspiring of Rabaey's undergraduate career. "In fact, they inspired me so much that I ultimately changed my personal direction from control systems to integrated circuits," Rabaey said. Gielen also feels that De Man's inspiring lectures and presentations are his most memorable trait. Claeys points out that even now as an emeritus professor, "his presentations are not at all a review of the history but more a look into the future. He is exploring new fields and tries to understand the physics involved, their challenges and potentials their may bring in the future."

Raebey recalls De Man was known to be a fair but hard-driving advisor. His undergraduate lab mates made a movie for a Christmas party of De Man's students slaving on the terminals in the computer room, spewing tons of computer paper from the printer, all this playing against the music of Ike and Tina Turner's "Proud Mary" with the lyrics "Working for De Man every night and day."

Gielen recalls, "the large size of the reading material for his courses. Hugo was infamous for that. He could motivate his students to work themselves through the big piles of difficult material that he was teaching."

Claeys notes, "He initiated the so-called 'student projects' whereby a group of 3 or 4 students had to work during the year on a dedicated project. In the 70s it was a new teaching concept which later became common practice."

Gielen recalls that De Man introduced many "design projects in our EE curriculum, where students could gain hands-on experiences with the course material. This includes also many projects with applying CAD software to VLSI design."

Claeys can still remember how an exam question of De Man's 35 years ago required undergraduates to examine the whole picture before designing a circuit solution. "I want to build a radio for my car and I have to drive through the Sahara, What type of technology should I use? You first had to analyze the question: the desert means a hot temperature, technology must reliable, before an answer could be given."

Claeys pointed out that De Man was available for the students when needed. "The assistants working for him and supervising laboratories also had to treat the students as a very valuable asset."

Claeys sums it up, "All his life he remained an enthusiastic professor who considered teaching as a very important job; I would more say a mission in his life. Working together with students was an extremely important issue for him."

"It is ironic, though, that De Man, despite being an inspired educator, never wrote a textbook himself about digital design. Some of his former students, like Jan Rabaey, have done so instead," notes Gielen.

De Man comments that a most satisfying part of his career has been seeing his Master and Ph.D. students contribute to progress in the field worldwide, both in the academic world and in industry. "For me, teaching is the most

rewarding profession as it provides you with the opportunity to multiply and transfer your knowledge and to help people to stimulate their own great creative talent and make it available to create a better society. I am extremely grateful to all of my students for this greatest of all presents!"

Seeing Clearly And Conveying It

One of DeMan's principles is that "if you cannot explain something in simple words you don't know about what you are speaking. Somebody can give high level technical presentations but often forget about basic things and concepts," Claeys recalls.

Claeys continues by noting that De Man would comment "many scientists are too much focused on their own narrow research field and the direct problems associated with them. Executing projects and attracting new projects are key for them. However, people should have a broad view and interest in order to put their own activities in the right context and take sufficient time to think about future trends and challenges. He is a great scientist with an excellent scientific track record but he also has a very good vision."

Rabaey agrees, "De Man is a real deep thinker - always listening and observing and from this distilling new visions. He also never stopped learning. As such, he has impacted the directions of many people and companies."

Georges Gielen continues, "De Man is essentially a visionary philosopher, who continuously looks ahead into the future (future applications and societal needs, state of the technology, etc.) and then tries to derive from that the research activities that need to be started today. The drawback of being a visionary though is that some of these tools were maybe commercialized a bit too early in time, in the sense that the market was not always mature enough for immediate wide adoption in industrial practice."

Sansen always remembers De Man's laid-back kind of style, always providing a very broad view on things. De Man has "a very broad view on where microelectronics is heading to; he continuously tries to extrapolate how technologies and system design can be teamed up towards higher complexity. Hugo deserves this prize as he has been one of the longest followers of Don Pederson," observes Sansen.

Sansen applauds De Man receiving the Pederson award as "he has surely been one of the most ardent followers of Pederson. He has been convinced all along that CAD software is essential to advance the design chips of high complexity. He has been in the forefront to illustrate this. And he has been very successful in putting out design software such that it could be used by designers; his 'meet-in-the middle' approach for system design has been exemplary."

Biography of Hugo De Man

Hugo De Man was born on September 19, 1940 in Boom, Belgium. He received the Electrical Engineering and Ph.D. degrees from the Katholieke Universiteit Leuven (K.U. Leuven), Belgium, in 1964 and 1968, respectively.

In 1968 he joined the K.U. Leuven, working on device physics and IC design. From 1969 to 1971 he was a postdoc at U.C. Berkeley, in the CAD group of Prof. D.O. Pederson. In 1971 he returned to the K.U. Leuven, where he became full professor in 1974.

In 1975 he was a Visiting Associate Professor at U.C. Berkeley. He was an Associate Editor for the IEEE Journal of Solid-State Circuits from 1975-1980 and Associate Editor for the IEEE Transactions on CAD from 1982 to 1985.

Prof. De Man has been advisor of 60 Ph.D. students. He has contributed to over 500 scientific publications and was keynote speaker at the ESSCIRC, DAC, DATE and ISSCC conferences. He was program chair of ESSCIRC and DATE conferences.

He is co-founder of the Interuniversity Micro-Electronics Center (IMEC) where, from 1984 to 1995, he was Vice-President of research on design methodologies for Integrated Telecom Systems. This group created the CATHEDRAL suite of silicon compilation tools DSP chips and the COWARE hardware-software co design systems. This work and the co-design of numerous telecom and multimedia chips have resulted in 6 Spin-Off companies.

In 1995 he became a Senior Fellow of IMEC working on system design technologies. His interests continue in Technology Aware Design methods and education methods for SoC design.

Prof. De Man received best paper awards at ISSCC, ESSCIRC, ICCD and DAC and the 1985 Darlington Award of IEEE Circuits and Systems Society. In 1999 he received the Technical Achievement Award of the IEEE Signal Processing Society, The Phil Kaufman Award of the EDA Consortium and the Golden Jubilee Medal of IEEE CAS. In 2004 he received the lifetime achievement awards of the European Design and Automation Association (EDAA) as well as the European Electronics Industry. Since 2005 he has been Emeritus of the K.U. Leuven and is still active as Senior Fellow of IMEC.

Prof. De Man is a Fellow of IEEE and a member of the Royal Academy of Sciences, Belgium.

Recipients of the IEEE Solid-State Circuit Awards

IEEE Donald O. Pederson Technical Field Award in Solid-State Circuits
2006 Mark A. Horowitz

IEEE Solid-State Circuits Technical Field Award
2005 Bruce A. Wooley
2004 Eric Vittoz
2003 Daniel Dobberpuhl
2002 Chenming Hu and Ping Ko
2001 No Award
2000 Robert H. Krambreck and Stephen Law
1999 Kensall D. Wise
1998 Nicky Lu
1997 Robert W. Brodersen
1996 Rudy J. van de Plassche
1995 Lewis M. Terman
1994 Paul R. Gray
1993 Kiyoo Itoh
1992 Barrie Gilbert
1991 Frank Wanlass
1990 Toshi Masuhara
1989 James D. Meindl

Solid-State Circuits Council Development Award
1988 Karl Stein
1987 Robert Widlar
1986 Barrie Gilbert
1985 Donald O. Pederson

IEEE Pederson Award Medal

The IEEE Solid-State Circuits Technical Field Award was created in 1989 and was renamed the IEEE Donald O. Pederson Technical Field Award in 2006. The awards before 1989 were Solid-State Circuits Council Award in Solid-State Circuits.

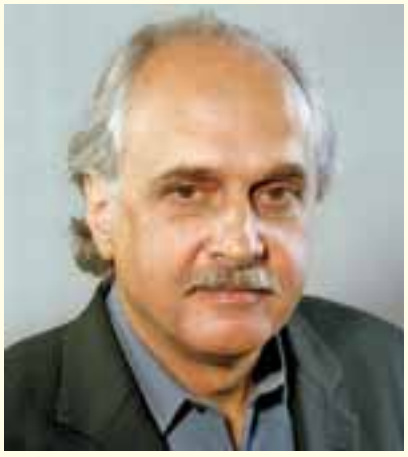
Pioneer in Mixed Signal Circuits will Receive IEEE Gustav Robert Kirchhoff Award at ISSCC 2007

Yannis P. Tsividis to be honored in February for contributions to circuits and MOS device modeling.

Katherine Olstein, SSCS Administrator, k.olstein@ieee.org

Yannis P. Tsividis will receive the IEEE Gustav Robert Kirchhoff Field Award for contributions to circuits and MOS device modeling at the plenary session of the ISSCC in San Francisco, CA on 12 February 2007. The Kirchhoff Award acknowledges outstanding contributions with long-term impact to the fundamentals of any aspect of electronic circuits and systems.

When Glenn E. R. Cowan, a Tsividis graduate student at Columbia University, recently applied for his first position after receiving the Ph.D., interviewers at IBM saw his work with Dr. Tsividis on mixed-signal VLSI computing as something "different from the mainstream" and gave him an equally challenging research job. A fellow student, Cowan recalled in a telephone interview, developed a Tsividis idea on parametric amplifiers using a MOS transistor as part of his Ph.D. project, presented it at ISSCC 2003, and won the conference best paper award.



"Like many EEs of my generation, I started as a child by building a crystal radio, and have been tinkering ever since." Yannis P. Tsividis

A Lifetime of Long Shots

Challenge and cutting-edge risk have characterized Dr. Tsividis's work throughout his career.

"I changed Ph.D. topics twice before I found one that excited me," he said in an email interview. "It was exactly the prejudice that MOS ICs are only good for digital that presented a challenge to me. I still recall an industrial visitor at Berkeley, who came to see what I was doing in my thesis work, and said, with some irony, 'So, you want to make amplifiers out of switches?'"

Today, the challenge of combining different domains is the approach to research that he enjoys most. "One of the pet projects in my group is continuous-time DSPs, with no sampling or aliasing – admittedly a long shot," he said.

Potential of Mixed Signal MOS Was Hard to Foresee

In the mid-seventies, it was diffi-

cult to get the idea of mixed signal MOS ICs accepted. "When Yannis began his graduate work around 1970," said Dr. Paul Gray, an early collaborator who is now Professor Emeritus and Professor in the Graduate School, EECS, UC Berkeley, in an email statement, "bipolar was used for virtually all analog integrated circuits and most digital circuits, which were at low integration levels at the time. MOS was used for memory and was just beginning to be used for some complex logic circuits." CMOS was in its infancy. "It was not easy to see that MOS technology would bring about the need to integrate both analog and digital on the same chip. This backdrop made MOS analog circuits a somewhat speculative proposition."

Career Breakthrough Was The First Useful MOS Operational Amplifier

"Working with Paul Gray, Yannis P. Tsividis developed and demonstrated the world's first useful MOS operational amplifier," said Dave Hodges, Professor of Engineering, EECS, UC Berkeley, via email. "It was fundamental to the development of mixed signal MOS integrated circuits, which provide vastly higher levels of circuit integration than bipolar analog devices," the prior mainstream technology.

Before CMOS was fully developed, the implementation of high gain op amps in NMOS was a real challenge, Hodges said. "Yannis came up with some circuit ideas to overcome this" using NMOS-only technology. Yannis's most lasting contribution to the usefulness of CMOS was his work on the adaptation of weighted-capacitor A/D conversion techniques to a special kind of converter used for voice, called a companding coder. He and others first demonstrated this technique, which became very widely used in telephone systems around the world in the 1980's and 1990's."

Kirchhoff Medal

Subsequent milestones, Tsividis said, have been "the work my students and I did on switched-capacitor circuit analysis and simulation; our techniques for automatically tuned integrated continuous-time filters; and our work related to precision MOS modeling for analog and mixed-signal design."

Dr. Tsividis, who is an IEEE Fellow, has received two best paper awards from the IEEE Circuits and Systems Society, as well as the IEEE-wide Baker best paper award.

Master Teacher

The recipient in 2005 of the IEEE Undergraduate Teaching Award, Dr. Tsividis is unusual among prominent researchers for his enthusiasm about teaching at this level. "I find it extremely rewarding," he said. "I have created a first-year undergraduate class, 'Introduction to Electrical Engineering,' where we mix circuits and electronics and attempt to make students tinker. The idea is to make them excited and motivated about what they will be learning in their follow-up classes. Just to show you how rewarding undergraduate teaching can be, let me tell you a story from that class. The class has a heavy lab component. During an experiment on amplifiers, a student comes to me and says, 'I see how, if I put a signal in, I get a signal out, and if I do not put a signal in, I get nothing out. What would happen if I took the output signal and used it as the input?' That student had re-invented oscillators right on the spot."

In order to reach undergraduates, a professor "must be willing to find ways to explain things intuitively to the students – not just throw a bunch of equations at them," Tsividis said. "The key is to make the math interesting, by making clear why it's useful. Dumping the first circuits class on anybody in an EE department has often had disastrous results in the motivation of students – I'm sure our field has lost some of the best minds because of this," he said.

Interdependence of Research and Teaching

"Whenever I want to really understand an area different from mine, I ask to teach a class in it," Tsividis said. "This is how I learned about DSPs, communications, signals and systems, and semiconductor devices. Only when I am forced to explain something carefully to others, do I understand it fully." As for his graduate students, he aims especially "to strike the right balance between helping them and challenging them to come up with their own solutions."

Shanthi Pavan, a recent Tsividis Ph.D., who is now an assistant professor at the Indian Institute of Technology in Madras, India, said in an email that he remembers especially Prof. Tsividis's "infectious enthusiasm," "clarity," "meticulous feedback," and "virtually limitless patience." Dr. Cowan would concur. "I don't think people can decide to become great teachers," he said. "It has to come from the heart." ■

Yannis Tsividis received the Bachelor's degree in electrical engineering from the University of Minnesota in Minneapolis in 1972, and the MS and Ph.D. degrees, also in electrical engineering, from the University of California at Berkeley in 1973 and 1976. He is Charles Batchelor Memorial Pro-

fessor of Electrical Engineering at Columbia University in New York, and has taught at the University of California, Berkeley, MIT, and the National Technical University of Athens.

Dr. Tsividis began his career by demonstrating the feasibility of MOS mixed-signal circuits. In 1976, at a time that MOS was considered a digital integrated circuit technology, he designed and built a fully integrated MOS operational amplifier and demonstrated its use in a PCM codec. These results were widely adopted by the industry in the first massively produced mixed-signal MOS ICs. Together with his students, he has since made many other contributions at the device, circuit, system and simulation level. These include techniques for fully integrated analog filters, which have been used in very large volume products such as disc drives and consumer electronics; switched-capacitor circuit theory and simulation, with the resulting software program Switcap widely used for such systems in the early days of MOS telecom ICs; companding analog filters; discrete-time parametric circuits; mixed analog-digital VLSI computation; and precision MOS device modeling, with benchmarks incorporated into IEEE standards for judging compact models. His book, "Operation and Modeling of the MOS Transistor" is a standard reference in the field. His most recent research effort involves 0.5 V analog/RF MOS circuits, and analog-inspired digital signal processing techniques, including continuous-time digital filters which operate without aliasing, and digital filters which use internal companding.

A Fellow of the IEEE, Dr. Tsividis is the recipient of the 1984 IEEE W.R.G. Baker Best Paper Award, the 1986 European Solid-State Circuits Conference Best Paper Award, the 1998 IEEE Circuits and Systems Society Guillemin-Cauer Best Paper Award, and the 2005 IEEE Undergraduate Teaching Award, and co-recipient of the 1987 IEEE Circuits and Systems Society Darlington Best Paper Award and the 2003 IEEE International Solid-State Circuits Conference L. Winner Outstanding Paper Award.

IEEE Educational Innovation Award to Fiez

TekBots® Named But Only Hint At Her Wide Ranging Talents

Terri Fiez, Chair of EE at Oregon State University, was presented with the 2006 IEEE Educational Activities Board Major Educational Innovation Award "for undergraduate engineering education innovation through creation and development of Platforms for Learning ® and its implementation in the electrical and computer engineering curriculum through the TekBots® program." Professor Fiez developed the program at OSU in Corvalis, Oregon over the last decade.

(l to r) Moshe Kam, IEEE VP Educational Activities, Terri Fiez, and Bruce Eisenstein, Awards Committee Chair Educational Activities, in New Orleans on 24 November 2006 during the BoD Meeting Series when Fiez received the Major Educational Innovation Award of the IEEE Educational Activities Board.

Dr. Jim Hellums, TI Fellow, who supervises funding of research at academic institutions, visits the Oregon campus and has watched many of the Platforms for Learning develop. TI funds a number of graduate research projects managed by Fiez today and has provided equipment for the program. "It would be easier to develop and launch a new program in industry than at a University because of the bureaucracy and inertia. Some people who didn't want to do it just don't. Even as a Department Head at a University one has to convince and cajole. It is a Herculean effort."

Hellums remembers that David J. Allstot, Fiez's graduate advisor at Oregon State University, predicted in 1988 that she would be a star. Terri had only completed her masters when she was first presenting her research report at ISSCC and Allstot had recommended that Hellums be sure to meet her because she was the best among the Allstot's graduate students.

Allstot, now Chair of EE at University of Washington, recalls that "From the time I first met Terri, it was clear that she was a ball of fire. She has a great personality and is naturally comfortable in the academic environment, whether as a student, professor, or administrator. Terri is equally good at strategic and tactical thinking."

Hellums recalled that Allstot had just proposed a robotics course at OSU in the 90s and had found no takers to expand the program

about the time he left OSU for Arizona. Fiez came on campus, took the course and grew the TekBot program, "got it done and made it successful. Then she enlarged the scope to the Platforms for Learning, which is all hers. It's her vision and excitement that gets it developed."

Allstot recalls, "I'm guessing here, but I don't think she got interested in robots until she became Head of ECE at OSU. There was a freshman robot course sequence that had been put in place at OSU one year prior to her arrival. It was based on the freshman robot course that CMU ECE had developed a few years earlier, but had some innovative additions including enrolling some students from the local high schools. But, it was just a start. The next step in the thinking, as I understand it, was to determine a way for those courses to impact the entire undergraduate curriculum. One idea was to involve seniors in capstone projects that improved the robots and alternatives to them for the freshman sequence would be developed, as well. Of course, this left the uncomfortable two-year robot-free gap between the Freshman and Senior years. This is the kind of situation where Terri shines. She conceived the "Platform for Learning" idea so that the first-year robot experience was continued throughout the undergraduate years, and centered around a central theme that motivated upper level classes. This meant adding capabilities to the Freshman robots such as wireless communications and control, etc. As is typical of Terri, she had a good idea and she found a way to describe it in very simple, but powerful terms that everyone could understand. This is really important for encouraging younger kids to get involved in Electrical Engineering."

"This also presented an opportunity for Terri to shine in another way. To be successful, she knew that significant resources would be needed to incorporate the Platform for Learning into their undergraduate curriculum. So, she presented the idea to Tektronix, Inc., and garnered critical support by adopting the 'TekBots' moniker for the program. On the surface, such a move might appear to be hype. However, it is far more significant than that. Previous to Terri's arrival, the Freshman Robot sequence culminated in a so-called 'Robot Rodeo' that was open to the general public, especially prospective students and their families. That term was almost pejorative, in my opinion, because it conjured up the old 'cow college' image that Oregon State had in the early days when it was Oregon Agricultural College. It certainly didn't suggest leading-edge high-technology education and research. With the simple twist of a phrase, TekBots, Terri conveyed the message that it was really leading-edge robot learning that had critical support from the local high-tech industry," recalls Allstot.

"She had a good idea and she found a way to describe it in very simple, but powerful terms, that everyone could understand."
Dave Allstot

Fiez emphasized that "this award really recognizes an amazing team. Over the last six years, we have had a core team of Don Heer (Education coordinator), Roger Traylor (senior instructor), Gale Sumida (Research and Education Support), Tom Thompson (Math and Science education PhD student and Philomath High School teacher). Together, it has been a thrill working with the faculty and students in our department to create a unique experience that addresses what seemed to be missing in our own educational experiences."

Nowadays, Hellums reports going to other schools and encouraging them to pick up the Platforms for Learning program. "I try to sell her idea." The TekBots Platform for Learning has been implemented in eight engineering courses at OSU at the freshman through senior levels and is used by five other institutions.

The concept includes two critical elements that aim to keep freshman and sophomores involved and staying in an EE program, Hellums reports. "It deals with the challenges of the major being too hard or too boring and gets over that sophomore hump," said Hellums. First robot implementations often end up looking like the OSU mascot – a Beaver with whiskers that sense objects and back up move around them. By working with applications of theory, sensing, seeing, reacting and moving, the students realize what engineers do in their career and see it can be fun. They also work in teams. Hellums recalls that there was nothing done in teams when he was a student but industry always works in teams, often fairly large teams. So the students learn early on to find their place in a team.

Kartikeya Mayaram, professor at Oregon State University, and a long time research collaborator with Fiez, sees definite differences in the graduate students who have come from the Learning Platforms curriculum. "They are ready to hit the ground running. They are already very good at trouble shooting. They have skills that enable them to do independent research and basically they are more resourceful in terms of knowing where to go and how to find information. That's a very valuable set of skills to come with to graduate school."

Allstot points out that as a researcher "Terri has made significant research contributions to oversampled data converters and substrate noise analysis techniques. She has made tremendous contributions to the high-technology industry by advising many students who are prepared to 'hit the ground running' in their jobs. She's made important educational innovations, and her impact at Oregon State cannot be overstated. She has done a lot at many different levels."

Mayaram outlines how Fiez's program has permeated much of the EE Curriculum. "Fiez is very involved with the Platforms for Learning and works with a core team examining the curriculum. They look for critical points that the curriculum would benefit from the platforms methodology, and develop a straw man proposal. So the core team does a lot of the ground work before they actually go and talk with the faculty. Then it's an interactive process at that point. Professor Roger Traylor who teaches the freshman introductory course, is already very involved in the TekBot program. They have a good idea of what's going on in a class and they make a proposal for what makes sense in particular labs. When the team has thought it out that well, it's a lot easier for the faculty to jump on board. The team takes on a lot of the detail work which can be a stumbling block if each faculty member is left on their own."

"Terri is natural leader. She is creative, full of new and innovative ideas. She is down to earth, values people and that makes a very nice work environment. In terms of research and mentoring her students she's a great person and her students love her. She keeps in touch with most of her graduate students long after they have graduated and been working for ages. She advises them even at later stages in their career," Mayram notes.

Allstot says, "Terri has it all. She is technically talented with a rare gift for leadership. Mark down this prediction: She will be a university president in the future. She is that rare star who is approachable and likable by all, mainly, I think, because it is always clear being around her that she really loves what she does. She has a great sense of humor that she uses effectively in her presentations and in person. Most important, she has a life. She is well balanced between her family and professional interests, more so than me and most of our colleagues."

Allstot asked Fiez, "Why do you obviously enjoy it so much?" Fiez replied, "I can't think of a more satisfying career. The opportunities for creativity, working with students to find their way, new technologies that will change the world, learning and laughing. I have been very lucky all throughout my career to work with wonderful people who are passionate about what they do. These include my graduate advisors, Gary Maki and Dave Allstot, and my graduate students, undergraduates, the faculty and staff in my School and Ron Adams, OSU Engineering Dean. I can't think of a day not filled with laughter!"

Dr. Terri S. Fiez

Terri S. Fiez ('82, M'85, SM'95, F'05) received the B.S. and M.S. degrees in electrical engineering from the University of Idaho, Moscow, in 1984 and 1985 respectively. In 1990 she received the Ph.D. degree in electrical and computer engineering from Oregon State University, Corvallis. From 1985 to 1988 she worked at Hewlett-Packard Corporation, in Boise and Corvallis. She was on the faculty at Washington State University from 1990 to 1999. In 1999, she joined the Department of Electrical and Computer Engineering at OSU as Professor and Department Head. She became Director of the School of Electrical Engineering and Computer Science in 2003.

Dr. Fiez has participated extensively in IEEE activities including: IEEE International Solid-State Circuits Conference (2000-2006), IEEE Custom Integrated Circuits Conference (1994-1998), IEEE Transactions on Circuits and Systems II Associate Editor (1995-1997), IEEE Journal of Solid-State Circuits Guest Editor (1997-1998) and IEEE CAS Distinguished Lecturer (2002-2004). Fiez received the National Science Foundation Young Investigator Award and the IEEE Solid-State Circuit Predoctoral Fellowship. She was elected Fellow of the IEEE in 2005 "for contributions to analog and mixed-signal integrated circuits."

16 New Speakers Will Diversify the SSCS Distinguished Lecturer Program

Sixteen outstanding members of SSCS have accepted the Society's invitation to join its Distinguished Lecturer Program. They are

Dennis Fischette
Ian Galton
Ali Hajimiri
Tadahiro Kuroda
John R. Long
Akira Matsuzawa
Sreedhar Natarajan
Bram Nauta
Clark T. C. Nguyen
Mehmet Soyuer
Mircea R. Stan
Toshiaki Masuhara
Ken Uchida
Albert J. P. Theuwissen
Roland Thewes
Ian Young

Each will serve a two-year term, from 1 January 2007 through 31 December 2008.

"The new additions to the DL list increase our representation in Asia and Europe to better serve the chapters in their respective communities," said C. K. Ken Yang, SSCS Education and DL Program Chair. "The list of DLs covers a broad range of current topics. Local chapters can leverage this resource for their activities and technical meetings," he said. The Society's DL Roster now totals 33 lecturers. It is available at sscs.org/Chapters/dl.htm.

Dennis Fischette is a Senior Member of the Technical Staff at Advanced Micro Devices (AMD) in Sunnyvale, CA. In 1986 he graduated from Cornell University, Ithaca, NY, with B.S. degree in Engineering Physics and then studied the History of Science at the Universi-

SSCS DLs Tour the IEEE Far East

Shanghai and Beijing Chapters Host Inaugural Programs on 15-18 November

Katherine Olstein, SSCS Administrator, k.olstein@ieee.org

The first SSCS Distinguished Lecturer Tour took place in the Far East (IEEE Region 10) on 15-18 November, 2006, immediately after the A-SSCC. The Shanghai and Beijing chapters each hosted a segment of the tour, which was initiated by SSCS DL Program Chair C.K. Ken Yang and coordinated by Dr. Zhihua Wang, Chair of SSCS-Beijing. The programs included presentations by Drs. Tom Lee, Vojin Oklobdzija, Betty Prince and Marcel Pelgrom.

"The SSCS Far East DL Tour in Shanghai was very successful," said Dr. Ting-Ao Tang, SSCS-Shanghai chair. "When we announced this activity, we received more than 100 return receipts asking to attend the workshop. On the afternoon of November 16th, 180 crowded the room."

The Society is planning a second Distinguished Lecturer tour in Europe (IEEE Region 8) for the fall of 2007.

In Beijing, an appreciative audience gathered to hear SSCS DL's Marcel Pelgrom and Betty Prince (left) and Tom Lee and Vojin Oklobdzija (at right). Dr. Zhihua Wang (center) hosted the event, which took place at Tsinghua University.

At Fudan University, Shanghai (from left): Professors Anquan Jiang, Huihua Yu, Yinyin Lin, and Ting-AoTang, with Vojin Oklobdzija, C.K. Ken Yang, Tom Lee, Betty Prince, and Prof. Zhiliang Hong.

ty of California, Berkeley. From 1988 to 1991 he worked for Integrated CMOS Systems Sunnyvale on device and circuit modeling. From 1991 to 1996 he worked for Hal Computer Systems, Campbell, CA on clock synthesizers and circuit design automation.

Before joining AMD, he worked for Chromatic Research, Sunnyvale on clock synthesizers, D/A circuits, and memories. His technical interests include PLL and DLL design, clock-and-data recovery, circuit analysis software, and high-speed IO circuits. He was a member of the ISSCC Digital Program Committee from 2001-2006 and created an online course on PLL Design for the IEEE Expert Now program in 2005. In his spare time, Dennis is an active jazz musician who recently performed in China and Vietnam.

Ian Galton received the Sc.B. degree from Brown University in 1984, and the M.S. and Ph.D. degrees from the California Institute of Technology in 1989 and 1992, respectively, all in electrical engineering. Since 1996 he has been a professor of electrical engineering at the University of California, San Diego where he teaches and conducts research in the field of mixed-signal integrated circuits and systems for communications. Prior to 1996 he was with UC Irvine, and prior to 1989 he was with Acuson and Mead Data Central. His research involves the invention, analysis, and integrated circuit implementation of critical communication system blocks such as data converters, frequency synthesizers, and clock recovery systems. In addition to his academic research, he regularly consults at several semiconductor companies and teaches industry-oriented short courses on the design of mixed-signal integrated circuits. He has served on a corporate Board of Directors, on several corporate Technical Advisory Boards, as the Editor-in-Chief of the *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, as a member of the IEEE Solid-State Circuits Society Administrative Committee, as a member of the IEEE Circuits and Systems Society Board of Governors, and as a member of the IEEE International Solid-State Circuits Conference Technical Program Committee.

Ali Hajimiri received the B.S. degree in Electronics Engineering from the Sharif University of Technology, and the M.S. and Ph.D. degrees in electrical engineering from the Stanford University in 1996 and 1998, respectively.

He has had appointments with Philips Semiconductors, Sun Microsystems, and Lucent Technologies (Bell Labs) in the past. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, where he is a Professor of Electrical Engineering and the director of Microelectronics Laboratory. His research interests are high-speed and RF integrated circuits.

Dr. Hajimiri is the author of The Design of Low Noise Oscillators (Boston, MA: Kluwer, 1999) and holds several U.S. and European patents. He is a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC). He has also served as an Associate Editor of the *IEEE Journal of Solid-State Circuits* (JSSC), an Associate Editor of *IEEE Transactions on Circuits and Systems* (TCAS): Part-II, a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD), Guest Editor of the *IEEE Transactions on Microwave Theory and Techniques*, and the Guest Editorial Board of Transactions of Institute of Electronics, Information and Communication Engineers of Japan (IEICE).

Dr. Hajimiri was selected to the top 100 innovators (TR100) list and is a Fellow of Okawa Foundation. He is the recipient of Caltech's Graduate Students Council Teaching and Mentoring award as well as Associated Students of Caltech Undergraduate Excellence in Teaching Award. He was the Gold medal winner of the National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, Netherlands. He was a co-recipient of the IEEE JSSC Best Paper Award of 2004, the International Solid-State Circuits Conference (ISSCC) Jack Kilby Outstanding Paper Award, two times co-recipient of CICC's best paper awards, and a three times winner of the IBM faculty partnership award as well as National Science Foundation CAREER award. He is a cofounder of Axiom Microdevices Inc. and member of SSCS AdCom.

Tadahiro Kuroda (M'88-SM'00-F'06) received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1999.

In 1982, he joined Toshiba Corporation, where he designed CMOS SRAMs, gate arrays and standard cells. From 1988 to 1990, he was a Visiting Scholar with the University of California, Berkeley, where he conducted research in the field of VLSI CAD. In 1990, he was back to Toshiba, and engaged in the research and development of BiCMOS ASICs, ECL gate arrays, high-speed CMOS LSIs for telecommunications, and low-power CMOS LSIs for multimedia and mobile applications. He invented a Variable Threshold-voltage CMOS (VTCMOS) technology

to control VTH through substrate bias, and applied it to a DCT core processor and a gate-array in 1995. He also developed a Variable Supply-voltage scheme using an embedded DC-DC converter, and employed it to a microprocessor core and an MPEG-4 chip for the first time in the world in 1997. In 2000, he moved to Keio University, Yokohama, Japan, where he has been a professor since 2002. He has been a Visiting Professor at Hiroshima University, Japan, and the University of California, Berkeley. His research interests include low-power, high-speed CMOS design for wireless and wireline communications, human computer interactions, and ubiquitous electronics. He has published more than 200 technical publications, including 50 invited papers, and 18 books/chapters, and has filed more than 100 patents.

Dr. Kuroda served as the General Chairman for the Symposium on VLSI Circuits, the Vice Chairman for ASP-DAC, sub-committee chairs for A-SSCC, ICCAD, and SSDM, and program committee members for the Symposium on VLSI Circuits, CICC, DAC, ASP-DAC, ISLPED, SSDM, ISQED, and other international conferences. He is a recipient of the 2005 IEEE System LSI Award, the 2005 P&I Patent of the Year Award, and the 2006 LSI IP Design Award. He is an IEEE Fellow and an IEEE SSCS Distinguished Lecturer.

John R. Long received the M.Eng. and Ph.D. degrees in Electronics from Carleton University, Canada in 1992 and 1996, respectively. He worked for 10 years at Bell-Northern Research, Ottawa (now Nortel Networks) designing ASICs for Gbit/s fibre systems, and for 5 years as a faculty member at the University of Toronto. He joined the faculty at the TU Delft in January 2002, where his current research interests include: low-power transceiver circuitry for highly-integrated radios and electronics design for high-speed data communications. Professor Long currently serves on the program committees of the ISSCC, ESSCIRC, IEEE-BCTM and GAAS 2004, and is a past Associate Editor of the *IEEE Journal of Solid-State Circuits*.

Toshiaki Masuhara (S'68-M'69-SM'90-Fellow'94), Association of Super-Advanced Electronics Technologies (ASET), was born on Mar. 5, 1945 in Osaka, Japan. He obtained B.S., M.S. and Ph.D. degrees in Electrical Engineering from Kyoto University, Kyoto, Japan in 1967, 1969 and in 1977, respectively. From 1969 to 1974, he was a member of the technical staff, 3rd and 7th Department at Hitachi Central Research Laboratory(CRL), Kokubunji, Tokyo, Japan, where he worked on depletion-load NMOS integrated circuits and on modeling of sub-threshold characteristics of MOS transistors. From 1974 to 1975, he was a special student, Department of Electrical Engineering and Computer Science, University of California, Berkeley where he worked on double-diffused MOS transistors and a new CMOS process. In 1975, he returned to Hitachi CRL and worked on new high speed CMOS SRAM. In 1987, he became department manager, 7th Dept., Hitachi CRL, developing memories, microprocessors, digital signal processors and high frequency silicon devices. He then became the manager of the 1st Dept. in 1990, performing research on high speed GaAs and bipolar ICs and materials. From 1991 to 1993, he was in Telecommunications Division, Hitachi, where he was responsible for the design of telecom ICs.He became General Manager, Technology Development Operation (Center) in 1993, General Manager, Semiconductor Manufacturing Technology Center, Semiconductor & IC Div. in 1997, and then became Senior Chief Engineer, Semiconductor Group, Hitachi. In 2001, he assumed his current position, Executive Director, MIRAI Project, Association of Super-Advanced Electronics Technologies (ASET).He is a member of IEEE and IEICE, Japan. He became a fellow of IEEE in 1994 with the citation, "For contribution in the invention and the development of NMOS circuits and high-speed CMOS memories". He was the program co-chair and the chair in 1992-, 1993-, and general co-chair and chair in 1996- and 1997-VLSI Circuit Symposium. He was an elected member of the Administrative Committee, SSCS from 1998 to 2000.He received IEEE Solid-State Circuit Technical Field Award on his contribution to NMOS depletion-load circuits and the development of high speed CMOS memories in 1990 and the IEEE third Millennium Medal in 2000. He has received a Significant Invention Award, Japan in 1994, four Significant Invention Awards, Tokyo, Japan in 1984, 1985, 1988 and 1992, Significant Invention Awards, Yamanashi, Japan in 1995 and Gumma, Japan in 1996.

Akira Matsuzawa received B.S., M.S., and ph. D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Matsushita Electric Industrial Co., Ltd. Since then, he has been working on research and development of analog and Mixed Signal LSI technologies; ultra-high speed ADCs, RF CMOS circuits, and digital read-channel technologies for DVD systems. From 1997 to 2003, he was a general manager in advanced LSI technology development center. On April 2003, he joined Tokyo Institute of Technology and he is a professor

on physical electronics. Currently he is researching in mixed signal technologies. He has published 30 technical journal papers and 50 international conference papers. He is co-author of 9 books. He holds 34 registered Japan patents and 65 US and EPC patents. He received the IR100 award in 1983, the R&D100 award and the Remarkable Invention award in 1994, and the ISSCC evening panel award in 2003 and 2005. He now serves SSCS AdCom members and he is an IEEE Fellow since 2002.

Sreedhar Natarajan is currently serving as the Founder & CEO of Emerging Memory Technologies (EMT) Inc. He founded EMT in Dec 2004, which in a short period has grown to become a successful leading design services and memory IP provider under his leadership. Prior to EMT, his industry experience comes from working at MoSys, Texas Instruments and Paradigm Technologies in the area of SRAM, DRAM, Memory Compilers and SOI. Mr. Natarajan serves on the Advisory Board of Diablo Technologies Inc, Solido Design Automation and HS Memory Inc. He also serves on various international conference technical committees like ISSCC, CICC, VLSI, ESSCIRC, ISLPED, SOC and VLSI Symposium. He co-authored the book "SOI Design: Analog, Memory and Digital Design" – Dec 2001, Kluwer Academic Publishers and is also the recipient of the IEEE Circuits and Systems Outstanding Service Award'01.

Dr. Natarajan was named among 'Top 40 under 40' individuals by the Ottawa Business Journal in 2005. This awards program honors individuals throughout the Ottawa business community that embody the region's entrepreneurial spirit and business acumen, while at the same time balancing community and charitable involvement. He has been a leading advocate to innovate and promote new memory technologies in the industry and is working with many academic and industry organisations to promote futuristic memory technologies. Mr. Natarajan obtained his Master's degree in computer engineering from University of Southwestern, Lafayette, LA. He is a IEEE Distinguished Lecturer for 2007-2008 and a Senior member for the Institute of Electrical and Electrical Engineers.

Clark T.-C. Nguyen received the B.S., M.S., and Ph.D. degrees from the University of California at Berkeley in 1989, 1991, and 1994, respectively, all in Electrical Engineering and Computer Sciences. In 1995, he joined the faculty of the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, to which he has very recently returned after a 3.5 year leave in Washington, DC, where he served as the MEMS Program Manager in the Microsystems Technology Office (MTO) of DARPA. His technical interests at Michigan focus on micro electromechanical systems (MEMS) and include integrated vibrating micromechanical signal processors and sensors, merged circuit/micromechanical technologies, RF communication architectures, and integrated circuit design and technology. Prof. Nguyen and his students at Michigan have garnered numerous Best Paper Awards at prestigious conferences, including the 1998 and 2003 IEEE Int. Electron Devices Meetings, the 2004 IEEE Ultrasonics Symposium, the 2004 DARPA Tech Conference, the 2004 IEEE Custom Integrated Circuits Conference, the 2005 IEEE Int. Solid-State Circuits Conference, and the 2005 IEEE Frequency Control Symposium.

In 2001, Prof. Nguyen founded Discera, Inc., a company aimed at commercializing communication products based upon MEMS technology, with an initial focus on the very vibrating micromechanical resonators pioneered by his research in past years. He served as Vice President and Acting Chief Technology Officer (CTO) of Discera from 2001 to mid-2002.

In mid-2002, Prof. Nguyen went on leave from the University of Michigan to join the Microsystems Technology Office (MTO) of DARPA in Arlington, Virginia, where he served as a Program Manager in MEMS technology. At DARPA, from mid-2002 through 2005, Prof. Nguyen created and managed a diverse set of programs that included Microelectromechanical Systems (MEMS), Micro Power Generation (MPG), Chip-Scale Atomic Clock (CSAC), MEMS Exchange (MX), Harsh Environment Robust Micromechanical Technology (HERMIT), Micro Gas Analyzers (MGA), Radio Isotope Micropower Sources (RIMS), RF MEMS Improvement (RFMIP), Navigation-Grade Integrated Micro Gyroscopes (NGIMG), and Micro Cryogenic Coolers (MCC).

Bram Nauta was born in Hengelo, The Netherlands, in 1964. In 1987 he received the M.Sc. degree (cum laude) in Electrical Engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies. In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands, where he worked on high speed AD converters. From 1994 he led a research group in the same department, working on analog key modules. In 1998 he returned to the University of Twente, as full professor heading the IC Design group in the MESA+ Research Institute and department of Electri-

cal Engineering. His current research interest is analog CMOS circuits for transceivers. He is also part-time consultant in industry and in 2001 he co-founded Chip Design Works. His Ph.D. thesis was published as a book: Analog CMOS Filters for Very High Frequencies, Kluwer, Boston, MA, 1993. He holds 8 patents in circuit design and he received the "Shell Study Tour Award" for his Ph.D. Work. From 1997-1999 he served as Associate Editor of IEEE Transactions on Circuits and Systems -II; Analog and Digital Signal Processing, and in 1998 he served as Guest Editor for IEEE Journal of Solid-State Circuits. In 2001 he became Associate Editor for IEEE Journal of Solid –State Circuits.

Mehmet Soyuer received the B.S. and M.S. degrees in electrical engineering from the Middle East Technical University, Ankara, Turkey, in 1976 and 1978. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 1988, subsequently joining IBM at the Thomas J. Watson Research Center, Yorktown Heights, NY as a Research Staff Member. His work has involved high-frequency mixed-signal integrated circuit designs, in particular monolithic phase-locked-loop designs for clock and data recovery, clock multiplication, and frequency synthesis using silicon and SiGe technologies. At IBM Thomas J. Watson Research Center, Dr. Soyuer managed the Mixed-Signal Communications Integrated-Circuit Design group from 1997 to 2000. He was the Senior Manager of the Communication Circuits and Systems Department from 2000 to 2006. In March 2006, he has been promoted to the position of Department Group Manager, Communication Technologies, at Thomas J. Watson Research Center. Dr. Soyuer has authored numerous papers in the areas of analog, mixed-signal, RF, microwave, and nonlinear electronic circuit design, and he is an inventor and co-inventor of eight U.S. patents. Since 1997, he has been a technical program committee member of the International Solid-State Circuits Conference (ISSCC). He was an Associate Editor of the IEEE Journal of Solid-State Circuits from 1998 through 2000, and was one of the Guest Editors for the December 2003 Special ISSCC Issue. Dr. Soyuer chaired the Analog, MEMS and Mixed-Signal Electronics Committee of the International Symposium on Low Power Electronics and Design (ISLPED) in 2001. He was also a technical program committee member of the Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF) in 2004 and 2006. Dr. Soyuer is a senior member of IEEE.

Mircea R. Stan received the Ph.D. and M.S. degrees in Electrical and Computer Engineering from the University of Massachusetts at Amherst and the Diploma in Electronics and Communications from Politehnica University in Bucharest, Romania.

Since 1996 he has been with the Department of Electrical and Computer Engineering at the University of Virginia, where he is now an associate professor. Prof. Stan is teaching and doing research in the areas of high-performance low-power VLSI, temperature-aware circuits and architecture, embedded systems, and nanoelectronics. He has more than eight years of industrial experience, has been a visiting faculty at UC Berkeley in 2004-2005, at IBM in 2000, and at Intel in 2002 and 1999. He has received the NSF CAREER award in 1997 and was a co-author on best paper awards at GLSVLSI 2006, ISCA 2003 and SHAMAN 2002. He is the chair of the VLSI Systems and Applications Technical Committee (VSA-TC) of IEEE CAS, was general chair for ISLPED 2006, technical program chair for ISLPED 2005, general chair for GLSVLSI 2003, and has been on technical committees for numerous conferences.

He has been an Associate Editor for the IEEE Transactions on Circuits and Systems Systems since 2004 and for the IEEE Transactions on VLSI Systems in 2001-2003. He has also been a Guest Editor for the IEEE Computer special issue on Power-Aware Computing in December 2003 and a Distinguished Lecturer for the IEEE Circuits and Systems Society for 2004-2005. Prof. Stan is a senior member of the IEEE, a member of ACM, IET, and also of Eta Kappa Nu, Phi Kappa Phi and Sigma Xi.

Albert J.P. Theuwissen was born in Maaseik, Belgium on December 20, 1954. He received the degree in electrical engineering from the K.U. Leuven, Belgium in 1977. His thesis work was based on the development of supporting hardware around a linear CCD image sensor.

From 1977 to 1983, his work at the ESAT-laboratory of the K.U. Leuven focused on semiconductor technology for linear CCD image sensors. He received the Ph.D. degree in electrical engineering in 1983. His dissertation was on the implementation of transparent conductive layers as gate material in the CCD technology.

In 1983, he joined the Micro-Circuits Division of the Philips Research Laboratories in Eindhoven, the Netherlands as a member of the scientific staff. Since that time he was involved in research in the field of solid-state

image sensing, which resulted in the project leadership of respectively SDTV- and HDTV-imagers. In 1991 he became Department Head of the division Imaging Devices, including CCD as well as CMOS solid-state imaging activities.

He is author or coauthor of many technical papers in the solid-state imaging field and issued several patents. In 1988, 1989, 1995 and 1996 he was a member of the International Electron Devices Meeting paper selection committee. He was co-editor of the IEEE Transactions on Electron Devices special issues on Solid-State Image Sensors, May 1991, October 1997 and January 2003, and of IEEE Micro special issue on Digital Imaging, Nov./Dec. 1998.

He acted as general chairman of the IEEE International Workshop on Charge-Coupled Devices and Advanced Image Sensors in 1997 and in 2003. He is member of the Steering Committee of the aforementioned workshop and founder of the Walter Kosonocky Award, which highlights the best paper in the field of solid-state image sensors.

During several years he was a member of the technical committee of the European Solid-State Device Research Conference and of the European Solid-State Circuits Conference.

Since 1999 he is a member of the technical committee of the International Solid-State Circuits Conference. For the same conference he acted as secretary, vice-chair and chair in the European ISSCC Committee and he is a member of the overall ISSCC Executive Committee.

In 1995, he authored a textbook "Solid-State Imaging with Charge-Coupled Devices". In 1998 he became an IEEE Distinguished Lecturer.

In March 2001, he became part-time professor at the Delft University of Technology, the Netherlands. At this University he teaches courses in solid-state imaging and coaches PhD students in their research on CMOS image sensors.

In April 2002, he joined DALSA Corp. to act as the company's Chief Technology Officer. In September 2004 he retired as CTO and became Chief Scientist of DALSA Semiconductors. This shift allows him to focus more on the field of training and teaching solid-state image sensor technology.

In 2005 he founded ETETIS (European Technical Expert Team on Image Sensors), a non-profit organization to promote European R&D activities in the field of solid-state image sensors.

He is member of editorial board of the magazine "Photonics Spectra", an IEEE Fellow and member of SPIE.

Roland Thewes was born in Marl, Germany, in 1962. He received the Dipl.-Ing. degree and the Dr.-Ing. degree in Electrical Engineering from the University of Dortmund, Dortmund, Germany, in 1990 and 1995, respectively. From 1990-1995, he worked in a cooperative program between the Siemens Research Laboratories in Munich and the University of Dortmund in the field of hot-carrier degradation in analog CMOS circuits.

Since 1994 he was with the Research Laboratories of Siemens AG and Infineon Technologies, where he was active in the design of non-volatile memories and in the field of reliability and yield of analog CMOS circuits. From 1997-1999, he managed projects in the fields of design for manufacturability, reliability, analog device performance, and analog circuit design. From 2000-2005, he was responsible for the Lab on Mixed-Signal Circuits of Corporate Research of Infineon Technologies focusing on CMOS-based bio-sensors, device physics-related circuit design, and advanced analog CMOS circuit design. Since 2006, he is heading a department developing DRAM Core Circuitry at Qimonda.

He has authored or co-authored some 120 publications including book chapters, tutorials, invited papers, etc., and he gave lectures and courses at universities. He served as a member of the technical program committees of the International Reliability Physics Symposium (IRPS), and of the European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF). He is a member of the technical program committees of the International Solid-State Circuits Conference (ISSCC), of the International Electron Device Meeting (IEDM), and of the European Solid State Device Research Conference (ESSDERC). Moreover, in 2004, he joined the IEEE EDS VLSI Technology and Circuits Committee.

Dr. Thewes is a member of the IEEE and of the German Association of Electrical Engineers (VDE).

Ken Uchida was born in Cambridge, MA in 1971. He received B.S. degree in physics, M.S. and Ph.D. degrees in applied physics all from the University of Tokyo, Tokyo, Japan, in 1993, 1995, and 2002, respectively. In 1995, he joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan. He has studied carrier transport properties in nano-scaled devices such as Single-Electron Devices, Schottky source/drain MOSFETs, Ultrathin-body SOI MOSFETs, Strained Silicon MOSFETs, and Carbon Nanotube Transistors. He developed the physics-based compact model of single-electron transistors and the design scheme of single-electron logic circuits. He investigated the physical mechanisms of mobility enhancement in uniaxial stressed

MOSFETs and clarified the importance of the effective mass change. In addition, he experimentally demonstrated the effectiveness of subband structure engineering in ultrathin-body SOI MOSFETs. Dr. Uchida is a member of the Japan Society of Applied Physics and IEEE Electron Devices Society. He won the 2003 IEEE EDS Paul Rappaport Award for his work on single-electron devices and 2005 Young Scientist Award from Ministry of Education, Culture, Sports, Science and Technology of Japan.

Ian Young was born in Melbourne, Australia. He received the BSEE in 1972, and the M. Eng. Science in 1975, specialized in Microwave Communications, from the University of Melbourne. He received the Ph.D. in Electrical Engineering from the University of California, Berkeley, in 1978, where he was one of the pioneers of the switched capacitor filter in MOS technology.

In 1983 he joined the Technology Development group at Intel Corporation, where he is currently an Intel Senior Fellow and Director of Advanced Circuits and Technology Integration. His technical contributions have been recognized in the design of DRAMs and SRAMs, process technology development and microprocessor implementations, the design of Phase Locked Loops for microprocessor clocking and high speed I/O and mixed-signal RF CMOS circuits for communications.

He was a member of the Program Committee for the Symposium on VLSI Circuits from 1991 to 1996, serving as the Program Committee Co-Chair/Chairman in 1995 and 1996, and the Symposium Co-Chair/Chairman in 1997/1998. He currently serves on the Executive Committee of the VLSI Symposia. Since 1992 he has been a member of the ISSCC Technical Program Committee, serving as the Digital Subcommittee Chairman from 1997 through 2003, Technical Program Committee Vice-chair in 2004 and Chair in 2005. Dr Young is an IEEE Fellow.

Congratulations New Senior Members

22 Elected in November

Alexandre Acovic	Switzerland Section	Antonio Leischner	Eastern Idaho Section
David Alexander	Albuquerque Section	Carl Lemonds	Central Texas Section
John Carpenter	Melbourne Section	Xiaopeng Li	Dallas Section
Gian-Franco Dalla Betta	Italy Section	Zhongmin Li	Eastern Idaho Section
Mark Durlam	Phoenix Section	Bjarne Malsnes	Norway Section
Luca Fasoli	Santa Clara Valley Section	Vasilis Papanikolaou	Toronto Section
Alkiviades Hatzopoulos	Greece Section	Luis Serrano	Spain Section
Stephen Horne	Central Texas Section	Chun-Meng Su	Hong Kong Section
William Hue	Oregon Section	Svein Tunheim	Norway Section
Tom Kjode	Norway Section	Walter Vollenweider	Switzerland Section
Chang-Ho Lee	Atlanta Section	Ming Zang	Twin Cities Section

TOOLS: How to Write Readable Reports and Winning Proposals

Part 2: Structure Your Reports to Please Your Reader

By Peter and Cheryl Reimold, www.allaboutcommunication.com

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One of the most daunting tasks of report writing is organization. How can you shape weeks of work into a single document? The key is to aim for ease of reading. The structure of your report should enable readers to get what they want as quickly and completely as possible. Here are two ways to do that.

The **scientific format** is good if you are addressing peers who may

Scientific Format	Management Format
Summary	Summary
Introduction	Introduction
Approach/Method	Conclusions
Discussion	Recommendations
Results	Results
Conclusions	Discussion
Recommendations	Approach/Method
Acknowledgments	Acknowledgments
Appendixes	Appendixes

want to evaluate the validity of your approach. It follows a logical progression, from an overview (summary) to the background (introduction), to your method, to a discussion of anything interesting that occurred, and then to your results. The conclusions and recommendations grow directly out of the results.

The **management format** uses the same categories but rearranges them to allow general management readers to get the information they want in the beginning, without having to read detailed sections.

You may not always need a section on method; this depends on the nature of your work and your readership. You may decide to give a more specific title to the discussion section if it covers only one topic. Otherwise, these sections work for most technical reports.

The **summary** provides the essence of your report, preferably in nontechnical terms. It should give general answers to all your readers' most urgent questions, but the primary reader here is usually the executive. Think broad brush strokes. A good outline for the opening summary is the PAW: Purpose, Achievement, What Next. For a discussion of the PAW, see the first column in this series (May/June 2002 Newsletter, p. 10).

The introduction explains what led to the work you did. It is an amplification of the purpose stated in the summary. To keep your introduction brief and interesting, consider your readers. How much background do they want and need? Tell them only that.

The **approach/method** opens with a summary of the key points of the method—points that could interest both management and technical readers. The rest of the section tells your technical readers how you proceeded.

The **discussion** requires informative subheadings. Use a clear subhead for each topic you explore. Open each topic with a summary paragraph that states your main message. Then consider which readers will be most interested in that topic. Note what questions they would have and try to answer them. If you have more to tell, state it after you have answered their questions, or put it in an appendix.

The **results** state simply what you found. It is best to present them as a bulleted list. (This stops you from adding long interpretations, which don't belong here.) For example:

- The five-pound roast was no longer on the counter.
- The dog was under the table, looking unwell.

The conclusions are your deductions from the results. They, too, work well as a bulleted list. They should grow clearly out of the results. For example:

- The dog ate five pounds of raw beef.

The recommendations state what to do next. They should grow directly out of your conclusions. For example:

- When preparing roast beef, close the kitchen door, making sure the dog is outside the kitchen.

The appendixes consist of material that is not critical for understanding your report but might be useful in the future. Make sure that each page has enough information on it to make it self-explanatory.

Finally, here are two points that apply to all sections:

1. In each section and subsection, move from the most to the least important information, unless some other logical scheme (e.g., chronology, left to right, top to bottom, causal sequence) clearly makes the section easier to understand.
2. Once you introduce several items in a certain order, stick to that order in the rest of the report.

Follow these simple rules, and your readers will thank you for making your report easily accessible and readable.

Cheryl and Peter Reimold have been teaching communication skills to engineers, scientists, and business people for 20 years. Their latest book, "the Short Road to Great Presentations" (Wiley, 2003), is available in bookstores and from Amazon.com. Their consulting firm, PERC Communications (1 914 725 1024), perccom@aol.com), offers business consulting and writing services as well as customized in-house courses on writing, presentation skills, and on-the-job communication skills. Visit their Web site at www.allaboutcommunication.com."

SSCS Awards $35,000 in Chapter Subsides

Katherine Olstein, SSCS Administrator, k.olstein@ieee.org

SSCS has awarded a record $35,603.96 in subsidies to a record 30 chapters for 2007-2008. The maximum allotment was doubled, in an AdCom vote last August, from $1000 to $2000 for single and new joint chapters, and from $500 to $1000 for established joint chapters.

Chapter subsidy awards are used primarily to fund distinguished lecturer seminars, chapter-level conferences and short courses and workshops. They also underwrite membership promotion, networking, and web development.

The chief events to be subsidized next year exemplify the range of benefits that chapters provide to local and regional IC professionals and students.

Chapter Workshops Foster Local Business Initiatives

In Shanghai, many IC design companies have sprung up, especially in SOC design and manufacturing. Therefore, the chapter is planning two seminars for spring, 2007 to introduce new methodologies to the IC community and to strengthen the relationship between academia and industry. As many as eighty attendees are expected at each event.

About 30 engineers from industry and academia will come together in a two-day workshop sponsored by the Finland/ Estonia chapter on 19-20 August, 2007. More information about this event, the seventh in a series, may be found at http://isc.dcc.ttu.ee/ws.htm.

Chapter Seminars Enhance Student Skills

SSCS-Bangalore, a chapter with 125 members, will devote SSCS subsidy funds to two one-day workshops for undergraduate and graduate students on advances and issues in devices and circuits. Each will take place at a local engineering college and involve faculty and students in addition to invited speakers. The Bangalore chapter subsidy will also help to fund the 10th VLSI Design and Test Workshop in cooperation with the VLSI Society of India on 10-13 August.

West Ukraine is planning "Pidstryhach Readings," a Regional Conference of Students and Young Scientists, and will also use SSCS subsidy funds to sponsor awards at the student scientific congress of the Institute of Telecommunications, Radioelectronics, and Electronic Engineering. SSCS-Sofia will conduct a competition in electronics design for high school students and support student activities at the Technical University of Varna.

In Novosibirsk, the SSCS student chapter and Novosibirsk-SSCS/EDS together sponsor the annual International Workshop and Tutorial on Electron Devices and materials (EDM). This event will take place for the eighth time in July.

The Society's new chapter in Pavia, Italy will use the SSCS subsidy to fund two two-day short courses in April and June on switched-capacitor filters, MEMS technology, data converters and microsensor interfaces for telecom, sigma-delta converters, and CMOS off-chip drivers. The courses will be approved for Ph.D. students by the Microelectronics PhD Course Advisory Board at the University of Pavia, and will also serve students from the Polytechnic University of Milan and the University of Genova and Parma, among other schools.

Chapter-Sponsored Annual Conferences Promote Regional Advancements

Sponsored by SSCS-Central Ukraine every year and aided by SSCS subsidy funds, the Crimean Microwave Conference (CriMiCo) regularly attracts 350 attendees in the fall. The West Ukraine chapter organizes the annual "Modern Problems of Radio Engineering, Telecommunications and Computer Science" (TCSET) conference and the International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED). The International Conference on Microelectronics (MIEL), sponsored by SSCS/ED-Serbia Montenegro with the aid of SSCS monies, annually draws an audience from over 30 countries in the spring. In Germany, two Multi Project Chip Workshops are held every year with the help of subsidy funds. Next year, the Novosibirsk Joint chapter will cosponsor the annual conference of the Russian A.S. Popov Radio Engineering Society.

Chapter-Sponsored Technical Meetings Educate Local Communities

Vancouver will use its first-ever subsidy award for five talks featuring three local and two invited speakers. The chapter hopes to double its membership during 2007 on the basis of these meetings and an upgraded website. The new Phoenix chapter is planning a local workshop in mid-February. SSCS-Ireland's subsidy will contribute towards the IEEE International Analog VLSI Workshop in Cork. SSCS-Hong Kong will present a "Symposium on Solid-State Devices and Novel Techniques for Biosensing Applications" next April. And the Novosibirsk Joint chapter will sponsor the first Russian IEEE Seminar on Solid-State Sensors, Actuators and Microsystems (MicroSys '2007) in December. It will also host a seminar on Nanotechnology in Electronics and participate in an All-Russia Chapter Chairs Congress.

More information about the SSCS Chapter Subsidies may be found at: sscs.org/Chapters/subsidy.htm. Information about the SSCS Extra Chapter Subsidy Program may be found at: sscs.org/Chapters/subsidy-extra.htm.

Far East Chapters Meet in Hangzhou, China

Inaugural SSCS Regional Meeting on 15 November, 2006

Jan Van der Spiegel, Chapters Committee Chair, jan@seas.upenn.edu

The first SSCS regional chapters' meeting was held in conjunction with the A-SSCC in Hangzhou, China on 15 November, 2006. The goal of the Far East meeting in IEEE Region 10 was to bring together chapter officers, society representatives and regional leaders to share experiences about best chapter practices, to provide information on chapter support services, and to stimulate further chapter development in Asia. The meeting was highly successful and resulted in a good dialogue among chapter and society representatives.

Professor Zhihua Wang of the Beijing Chapter hosted the event and made the local arrangements which ensured a very smooth and well run meeting. Six chapters were represented:
Beijing Chapter (Prof. Z. Wang)
Hong Kong Chapter (K-P. Pun)
Seoul Chapter (J. Chung and S-I. Lim)
Singapore Chapter (Y-P. Xu)
Shanghai (T.A. Tang) and
Taipei Chapter (H-S. Lin).

Several SSCS Society representatives attended: R. Jaeger (President of the SSCS), Jan Van der Spiegel (Chapters Chair), Ken Yang (Chair of the Education Committee) and Anne O'Neill (Executive Director). In addition, three Far East dignitaries were present: Nicky Lu (A-SSCC Steering committee and Technical Program Co-Chair), C. K. Chang (A-SSCC Steering Committee), and X. Yan (Dean, EE College of Zhenjian University). Also, two Distinguished Lecturers participated: Betty Prince and Vojin Oklobdzija.

After the luncheon, Professor R. Jaeger welcomed all participants, congratulated the chapter chairs on an outstanding job and stressed the important role chapters play in bringing educational and professional benefits to the local membership. Professor Van der Spiegel gave an overview of SSCS Chapter growth and activities in Region 10. Professor Ken Yang talked about the Distinguished Lecture Program and the DL tour in Region 10 immediately following the A-SSCC, on 15-18 November. Anne O'Neill reviewed administrative aspects, educational opportunities and financial aspects of chapters. During the remainder of the meeting, chapter representatives gave brief overviews of their respective chapter activities. The meeting concluded with a boat tour on the beautiful West Lake, followed by a traditional Chinese dinner.

The Society plans to hold a second regional chapter meeting in September, 2007 in conjunction with ESSCIRC.

From left, Kong-Pang Pun of The Chinese University of Hong Kong, Voijin Oklobdzija of University of Sydney , Betty Prince of Memory Strategies International, C.K. Ken Yang of UCLA, Yong Ping Xu of the National University of Singapore, Zhihua Wang of Tsinghua University, Ting-Ao Tang of Fudan University, Richard C. Jaeger of Auburn University, Anne O'Neill of IEEE SSCS, Andy Jinyong Chung of Puhang University of Science and Technology, Jan Van der Spiegel of University of Pennsyvlania, C. K. Wang of National Taiwan University, Nicky Lu, of Etron Technology, Shin Il Lim of Korea's Ministry of Commerce, Industry and Energy, and Hsung- Hsien Lin of National Taiwan University.

V. Oklobdzija Offers IEEE DL Talk and Keynote Address to PEECS Symposium in Western Australia

Microprocessors in the Past and Future Explored at November Meetings

By Adam Osseiran, Edith Cowan University, a.osseiran@ecu.edu.au

Professor Vojin Oklobdzija, an IEEE Fellow and Distinguished Lecturer of the IEEE Solid-State Circuits Society gave a seminar entitled "Future of Microprocessors: Retrospective and Challenges" to the electronic and computer communities in Western Australia on Monday, 6 November, 2006. The venue was the Innovation Centre WA at the Technology Park in Bentley. Twenty five researchers and professionals from Perth attended the lecture.

From left, Dr. Vojin Oklobdzija, Dr. Adam Ossieran, and Dr. Lance Fung.

In his talk, Professor Oklobdzija presented a retrospective of modern microprocessor development. He addressed advances in enabling technology that have brought unprecedented growth and gave a perspective for future development. The features which have enabled the development of modern microprocessors, guiding principles and contributions made by modern microprocessor architecture were discussed, as well as the move into super-scalars with respect to performance and implementation difficulties.

Professor Oklobdzija then addressed the one billion transistor challenge and the impact of the computer entry into consumer market, representing new potentials and new challenges. An interesting discussion between Professor Oklobdzija and the participants, and among the participants themselves, followed the talk and continued outside at a reception in his honor provided by the IEEE local section.

On the next day, Professor Oklobdzija gave the keynote address "Directions in Computer Engineering" at the 7th Post Graduate Electrical Engineering Computer Symposium (PEECS) for researchers and postgraduates from the four Western Australian Universities. The Symposium was organized by Associate Professor Lance Fung, who is the IEEE Western Australia Section Chair. More than 100 participants filled the auditorium.

Professor Oklobdzija put the computer engineering discipline into a historical perspective and showed how computers have seen an unprecedented expansion since the first electronic computers were built some 50 years ago. He later explained how computers are playing a major part in our lives and are fuelling economic growth. He then outlined major milestones and achievements in computer development and continued by showing trends and sharing his view on where growth and expansion in this area may be expected. At the end, he offered some recommendations for the university computer engineering programs.

The visit of Professor Oklobdzija to Western Australia concluded with a discussion about a proposal to initiate a new joint IEEE chapter of SSCS and EDS, which should become two distinct chapters later. Current developments in the research communities in Western Australia in the fields of microelectronics, photonics, solid states and electron devices with new nanotechnology and nanomaterial for applications such as military, medical, and general sensing applications justify the establishment of a new IEEE chapter.

Denver Hosts Technical Seminars on Cutting-Edge CMOS Technology and High-Speed Test

Alvin Loke, Denver Chapter Chair, alvin.loke@ieee.org, Bob Barnes, Denver Chapter Vice Chair & Treasurer, bob_barnes@ieee.org, Tin Tin Wee, Denver Chapter Secretary & Webmaster, tintin.wee@ieee.org

In the past year, the Denver SSCS Chapter hosted eight monthly seminars, including four by SSCS Distinguished Lecturers. These talks spanned a variety of exciting developments in IC design, cutting-edge CMOS technology, and high-speed test.

In the first seminar of 2006, Dr. Victor Chan of IBM gave a very informative overview of state-of-the-art strain and substrate engineering techniques to enhance channel mobility in bulk and SOI CMOS. In February, Dr. Osvaldo Buccafusca of Avago Technologies, who is also the Chair of the IEEE Centennial Subsection that covers northern Colorado and southern Wyoming, described the challenges and implementation of a very high-speed optical sampling oscilloscope for characterization of optical serial links. Adam Healey of Agere Systems, Chair of the IEEE 802.3ap Standards Committee, built on this theme with a discussion of 10 Gigabit Ethernet over backplane interconnects. This topic is of significant interest to the many Fort Collins IC designers dealing with high-speed electrical data links. Stefan Rusu presented the next talk on Intel's Dual-Core Xeon® Processor. Abstracts and slides for all lectures are available at the Chapter's website.

Alvin Loke, Denver Chapter Chair, presented an award of appreciation to Dr. Pelgrom.

Dr. Marcel Pelgrom of Philips Research visited Fort Collins in May to deliver our first Distinguished Lecture of the year. A pioneering expert on transistor variability, he delivered an insightful talk on the analog challenges associated with nanometer CMOS. Given its relevant nature, Dr. Pelgrom's seminar drew a chapter record attendance of 120!

The next DL seminar was given by Dr. Kiyoo Itoh of Hitachi Central Research Laboratory, who spoke about ultra-low voltage nano-scale embedded RAMs. Dr. Itoh emphasized the importance of fully-depleted SOI technology as an enabling solution to overcome device mismatch and allow for ultra-low voltage operation. Prof. Boris Murmann was the next speaker, coming from Stanford University to discuss the importance of digital techniques to compensate for analog limitations, such as nonlinearity and variability, in sub-100nm CMOS.

In August, Prof. Behzad Razavi visited from the University of California at Los Angeles. His much anticipated seminar covered some exciting new developments on the 60GHz RF CMOS transceiver front and discussed design and modeling challenges in that domain. Not surprisingly, Prof. Razavi's renowned authorship drew quite a trail for autographs. Thanks to members-at-large Herman Pang and Michael Gildorf of Avago Technologies for making possible our first ever seminar recorded on DVD. The DVD will be available to chapters, upon request.

Following a social event in November, the year ended with a ninth lecture by Sam Naffziger of Advanced Micro Devices, who spoke on high-performance processors in a power-limited world. Fort

The Distinguished Lecturer seminar by Dr. Marcel Pelgrom attracted an audience of 120 at Fort Collins, CO on 11 May 2006.

The Society distributed this DVD as a technical treat to attendees at the Society's Far East Chapters Luncheon and Meeting in November.

Herman Pang (far left) and Mikail Gilsdor (second from right, second row) video taped Dr. Razavi's talk on 1 August, 2006. Dr. Razavi is eighth from right, front row. A. Loke and Tin Tin Wee, Chapter Secretary and Webmaster, are to his right.

Collins has quickly become a hotbed of leading-edge microprocessor activity with AMD recently opening its brand new Mile High Design Center to match Intel's established presence in Itanium development.

We regret to announce that Past Chair Dr. Don McGrath decided to step aside from chapter activities, having been overwhelmed by his responsibilities at LSI Logic. We wish to extend our best wishes to him and heartfelt thanks for his instrumental leadership and commitment to grow this young chapter for several years soon after its inception in late 2002. We are also grateful to our past speakers, especially those who traveled from distant places and undoubtedly busy schedules to support our humble service to the northern Colorado design community. Finally, we welcome Bruce Doyle who recently joined the existing officer team.

Please visit ewh.ieee.org/r5/denver/sscs/ for more information, including past presentation slides, about our chapter events.

The Second A-SSCC Considers Challenges for the e-Life

Gathered for the opening plenary of the A-SSCC in Hangzhou are(l-r) Prof Tadahiro Kuroda of Keo University and Chair of the Invited Program Committee, Nicky Lu of Etron Technology and Chair of Conference Industry Program, Richard C. Jaeger of Auburn University and President SSCS, Richard Chang, the President of Semiconductor Manufacturing International Corporation and Chair of the Technical Program, and C.K. Wang of National Taiwan University and Conference Steering Committee Chair.

The successful Asian Solid-State Circuits Conference in November, 2006 in Hangzhou, China was organized with a core of 107 papers selected by an international program committee. The acceptance rate was 32% with a conference audience of 260 registered attendees. CK Wang, the Steering Committee chair of A-SSCC, reported that the conference was quite successful both "in terms of paper quality and foreign attendees with 82 from Japan, 48 from Taiwan, and 39 from Korea." Prof Wei of Tsinghua University and local host felt that it was the first high quality and world class conference held in China. The tutorials that began the conference were open at no cost to any students in attendance.

Three papers, announced as winners of the Student Design Contest, were awarded at A-SSCC. The competition, in cooperation with the ISSCC, includes transportation for the lead student researcher to the ISSCC February 2007 in San Francisco, for the papers to be included in the ISSCC poster session. The A-SSCC student design contest finalists are selected from regular accepted papers that are authored by students. Only the realized designs, not simply simulations, are selected and invited to demonstrate the operation of the chips on-site. It is not a contest with a single specification or application, but rather a contest for the completeness of development and demonstration of the fabricated integrated circuit. The papers, co-authors, and abstracts are listed below.

(I) A TCAM-based Periodic Event Generator for Multi-Node Management in the Body Sensor Network
Sungdae Choi, Kyomin Sohn, Jooyoung Kim, Jerald Yoo and Hoi-Jun Yoo (KAIST)

A low-power periodic events generation is essential for a node controller in the network system with centralized control and the timer interrupt generation for various devices in a CPU. The proposed TCAM-based periodic event generator manages the issuing events with the programmed value and the number of the events is equal to the number of the word line of the TCAM block. The NAND-type TCAM cell operates with as low as 0.6V supply voltage and the low-energy match line precharge reduces the search line transition which causes most of the search energy dissipation. The implemented event generator consumes 184-nJ energy to schedule events of 255 nodes for 24-hours, which is less than 10% of energy consumption of conventional hardware timer blocks.

Winners of the A-SSCC 2006 student design contest were (from left) first, Sungdae Choi of KAIST, Seoul, second Mr. Yusaku Ito of the Tokyo Institute of Technology, and third Mr. Simone Gambini Simone Gambini and Jan Rabaey of the University of California at Berkeley. Presenting the awards is Prof. Hoi-Jun Yoo, Chair of Design Contest.

(2) A 0.98 to 6.6 GHz Tunable Wideband VCO in a 180 nm CMOS Technology for Reconfigurable Radio Transceiver

Yusaku Ito, Hirotaka Sugawara, Kenichi Okada and Kazuya Masu (Tokyo Institute of Technology)

This paper proposes a novel wideband voltage-controlled oscillator (VCO) for multi-band transceivers. The proposed VCO has a core LC-VCO and a tuning-range extension circuit, which consists of switches, a mixer, dividers, and variable gain combiners with a spurious rejection technique. The experimental results exhibit 0.98-to-6.6GHz continuous frequency tuning with -206dBc/Hz of FoMt which is fabricated by using a 0.18um CMOS process. The frequency tuning range (FTR) is 149%, and the chip area is 800µm x 540µm.

(3) A 1.5MS/s 6-bit ADC with 0.5V supply

Simone Gambini and Jan Rabaey (University of California at Berkeley)

A moderate resolution analog-to-digital converter targeting wireless sensor networks applications is presented. Employing a successive-approximation architecture, the device achieves 6 bits of resolution at 1.5 MS/s output rate, while drawing 28 microamps from a low 0.5 V supply, corresponding to a Figure of Merit (FOM) of .25pJ/conversion step. Low-density metal5-metal6 capacitors guarantee feedback DAC linearity while minimizing input capacitance, while the use of a passive sample and hold, combined with a class-AB comparator reduce analog power dissipation to 4 microWatts (30% of the total). The analog core is operational for supply values as low as .3V, even though sampling rate is reduced to 175kS/s.

Invitation from the ISSCC 2007 Technical Program Chair

I would like to invite you to attend the 54th ISSCC which will be held in San Francisco on February 11-15, 2007. The conference theme is "**The 4 Dimensions of IC Innovation**," in recognition of the emerging synergisms between the various aspects of integrated circuit realization. There will be 243 outstanding papers distributed over 31 technical sessions covering advances in analog and digital circuits, data converters, imagers, display and MEMS, memories, RF building blocks, technology directions, and wireless and wireline communications. A common theme among many of the papers is how to control power consumption in deep-submicron technologies while pushing for higher performance and functionality. This requires careful optimization among the four dimensions of IC design (technology, devices, circuits, and architecture). Several papers will present new approaches or circuits for dealing with the power issue, while other papers will set new performance records.

Besides the regular paper sessions, the ISSCC will offer a wide variety of high-quality educational programs, adding to the already significant value of the ISSCC. This

year, there are ten Tutorials, seven Design Forums, and one Short Course. This year's short course deals with the popular topic of "*analog, mixed-signal, and RF circuit design in nanometer CMOS*".

There are also three excellent plenary presentations. Morris Chang of TSMC will talk about the future and the challenges of silicon foundries and how foundries will continue to be a driving force for the semiconductor industry by providing advanced technologies. The second plenary presentation by Lewis Counts of Analog Devices will focus on analog and mixed-mode circuit innovation in the nanoscale regime. The third talk by Dr. Joel Hartmann of Crolles2 Alliance will explain how increased parameter variability in today's nanoscale technologies requires a global optimization among the four dimensions of IC design.

There are also the traditional evening sessions. One of the evening panels will discuss the "*ultimate limits of ICs*" while another will deal with "*digital RF*". The panels bring together experts and visionaries who share their views with the participants. In addition, seven special topics sessions will provide an opportunity to learn about an emerging topic in a relaxed setting.

As you can see, the upcoming ISSCC continues its tradition of presenting the best in solid-state circuits and providing an opportunity to learn about the latest developments through its rich choice of educational activities. In addition, the ISSCC is a great avenue to network, meet old colleagues and make new friends. I am sure you'll enjoy the ISSCC and I hope to be able to welcome you in San Francisco.

Jan Van der Spiegel
Technical Program Chair, ISSCC 2007
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Solid-State Circuits Conference Will Focus on Nano-Era Synergy

ISSCC 2007 to Meet on 11-15 February in San Francisco

Katherine Olstein, SSCS Administrator, k.olstein@ieee.org

Synergy between various dimensions of integrated circuits in the nano-electronic era will be the theme of ISSCC 2007. ISSCC is the flagship conference of the Solid-State Circuits Society.

Balance Among Process, Circuit, Architecture, and System Technology Advances Required for Innovation

Pushed by the continued growth of Moore's Law, integrated circuits have evolved from the micro-electronic into the nano-electronic era. This transition has created tremendous opportunities for higher-density, higher-performance, lower-power circuits and systems resulting in cost-effective solutions for ubiquitous communications, computation, sensing, display, consumer electronics, and multimedia. However, the advent of the nano-era has blurred the traditional boundaries between the four dimensions of IC innovation (technology, devices, circuits, and system architecture). As a result, innovation in solid-state circuits requires an intricate balance among advances in process, circuit, architecture and system technology.

Novel Circuit Concepts and Four-Dimension Interrelationships Selected for Technical Program

Paper proposals for novel circuit concepts and systems and explorations of the interrelationships among the four dimensions of IC innovation were especially sought for the Conference.

Within the resulting technical program of 234 papers, fifty percent are devoted in nearly equal proportions to wireline, digital, wireless, and the combined category of imagers, medical, MEMS and displays. Special topic sessions in three of these technical areas will be "Last-Mile Access Options: PON/DLS/Cable/ Wireless," "Secure Digital Systems," and "Implantable and Prosthetic Devices: Life-Changing Circuits." The Wireless session will include a panel discussion entitled "Digital RF– A Fundamentally-New Technology, or Just Marketing Hype?" and a forum, "Giraffe: Power Amplifiers and Transmitter Architectures." There will also be a tutorial within each area.

In the area of data converters we notice a shift into the 90nm regime with 1-1.2V supply voltage giving rise to higher performance and lower power consumption for multimode operations. The papers in the digital arena showcase 65nm technologies at clocking speed up to 5GHz. Power management receives special attention among the high performance digital papers. Circuits make further inroads into the medical area with implantable brain probes, multi-channel high-resolution retinal prosthesis. CMOS imagers witness continued shrinking of the pixel size while improving performance, competing with CCD type of imagers. Papers in the area of Technology Direction will showcase the next-generation, post-CMOS technologies and systems.

Special-Topic Sessions on Next-Generation Circuit Design

On Sunday evening before the first day of the Conference, two special-topic seminars addressing next-generation circuit-design challenges will be open to all attendees.

"Digitally Enhanced Analog and RF" will include four talks by Boris Murmann (Stanford University), Steve Lewis (UC, Davis), Larry Larson (UC, San Diego) and Jan Craninckx (IMEC, Belgium), who will explore challenges and trends in CMOS in scaling technologies:

As CMOS chip technologies scale to finer line widths, smaller devices, and lower voltages, analog circuit targets are harder to achieve due to larger device mismatch, non-ideal device characteristics, and limited voltage swing. At the same time, scaled technologies reduce power and area, while increasing performance and lowering cost for digital circuits every year. These trends lead to the displacement of high linearity, highly accurate analog circuits by lower performance analog circuits. However, digital signal processing techniques come to the rescue, resulting in better performance, at lower cost and shorter design time.

"Circuit Design in the Year 2012" will be presented by David Frank (IBM, TJ Watson, Yorktown Heights, NY), Hae-Seung Lee (MIT), Marcel Pelgrom (Philips Research, Eindhoven, The Netherlands) and Borivoje Nikolic (UC, Berkeley). This special-topic-session will provide a thorough overview of special circuit design considerations which will accommodate sub-32nm device idiosyncrasies. Four experts will share their insight into issues confronting microprocessor and mixed-signal design in 2012 and offer potential solutions.

Short Course for Entry-Level and Experienced Nanometer CMOS Designers

A Short Course organized by Ian Galton entitled "Analog, Mixed-Signal and RF Circuit Design in Nanometer CMOS" will be offered twice, with staggered starting times. Instructors Matt Miller (Freescale

Semiconductor), Bram Nauta (University of Twente, The Netherlands), Robert Bogdan Staszewski (Texas Instruments), and Michel S. J. Steyaert (Katholieke Universiteit, Leuven, Belgium) will each give a lecture.

In this one-day session they will explain the fundamental limitations faced by those designing critical communication system blocks such as amplifiers, mixers, data converters, and phase-locked loops in nanometer CMOS, and present state-of-the-art circuit and system-level techniques for addressing these limitations. A DVD including (1) The visuals of the four Short-Course presentations in PDF format; (2) Audio recordings of the presentations along with written transcriptions; (3) Bibliographies of background papers for all four presentations; and (4) PDF copies of selected relevant background material and important papers in the field (10 to 20 papers per presentation) may be purchased at registration time, or at the on-site registration desk. A substantial price reduction is offered to those who attend the course.

Plenary Session

At the opening of the conference, three invited speakers from industry will examine key considerations and offer roadmaps for technical innovation.

"*Foundry Future: Challenges in the 21st Century*" will be the topic of Morris Chang, Founding Chairman, Taiwan Semiconductor Manufacturing Corporation, Hsinchu, Taiwan.

The foundry business-model is an important positive influence on the health of the overall IC industry. Therefore, it is critically necessary to scan the future for potential issues that might inhibit foundry-industry growth.

In order to ensure continued expansion, the foundry industry must address two significant challenges: The first and foremost challenge is business growth: We anticipate that growth matching previous industry experience may be more difficult to attain in the future, simply because revenue growth of the semiconductor IC industry (as a whole) has slowed since 2000, and will continue to do so. Additionally, the penetration of the CMOS-logic market by the foundry industry cannot continue unabated indefinitely; saturation should be anticipated in the future.

The second challenge for the foundry industry is to maintain profitability: The growth of the industry has attracted many companies to offer foundry services. Consequently, competition between these companies increases the potential for commoditization of foundry services, where many foundries, with apparently similar (but substantively different) services, compete on the basis of price alone.

The foundry industry must respond to these challenges by two means: expanding into new IC-product markets enabled by the cost reduction and performance increases resulting from technology scaling; and by penetrating segments of the IC market that are currently not involved in foundry relationships, by broadening the range of technologies that are offered. In the future, circuit designers can expect, therefore, to be able to access process technologies tuned in various ways: For memory, analog, high-performance-logic, or image-sensor applications, as well as for CMOS logic.

Lewis Counts, Vice-President of Analog Technology and Fellow Analog Devices, Wilmington, MA, will discuss "*Analog and Mixed-Signal Innovation: The Process-Circuit-System-Application Interaction.*"

Innovation in analog and mixed-signal electronics becomes increasingly more important to the continued growth of the IC industry. While technologists working in the analog and mixed-signal arena share, with their digital counterparts, the overarching goal of reducing power and cost-per-function in each IC generation, they must also operate under physical constraints that, until recently, have been secondary in the digital world.

From the advent of the first analog IC, analog designers have exploited the potential of process technology to develop circuits that minimize the impact of variation in process parameters on product performance. While process scaling has enabled the development of a wide variety of products, from cellphones to advanced medical-imaging systems, the success of these products depends in large measure on their ease of use, and seamless connection to wireless and wired networks. Analog and mixed-signal subsystems, including display drivers, and WLAN and cellular radios, support these critical interfaces. The downward scaling of supply voltage in deep submicron CMOS (now at 1V), may limit dynamic range, forcing some analog functions to be implemented on other processes, but it has also enabled new circuit architectures that gain back dynamic range.

The creative combination of process, design, and system architecture in providing robust solutions for demanding applications, will prove to be even more crucial in the future. Such solutions will be essential in meeting the challenges posed by the physical realities of deep- submicron design in achieving gigahertz speeds, minimizing power consumption, and integrating multiple functions in smaller packages.

Joel Hartmann, Director, Crolles2 Alliance, STMicroelectronics, Crolles, France will explore the intricate balance that will increasingly be required among process, device, circuit, and system aspects of design in "*Toward a New Nanoelectronic Cosmology.*"

Gone forever are the days of smooth roadmap scaling, with its more-or-less-simple design rules, adequate supply voltages, and unimpeded circuit shrinkage. As

scaling moved ahead to nanometer dimensions, things changed: Devices became more difficult to predict, and global performance degraded due to leakage and dispersion. One of the consequences of this deteriorating situation has been that increased parameter variability has led to a significant mismatch between simulation and actual measurement results, at all levels. While many of these effects have already been well known to analog designers, the surprise, now, is that they are more broadly important, even in digital design, where previously available noise margins have almost disappeared.

Clearly, deep understanding and modeling of all underlying physical causes is urgently required to guide the right choices at all levels. Conceptually, such understanding will lead to acceptable levels of performance, manufacturability, and yield, at ever-decreasing feature sizes. Meanwhile, the increased parameter variability observed today, as one technology node invites the next, reveals the tight coupling of the four seemingly- independent dimensions of design, motivating the need to configure a new nano-cosmology, one in which global optimization results only from an intricate balance between the Process, Device, Circuit, and System aspects of design.

In this new nano-cosmology, the emerging concept of Generalized Design-for-Manufacturability (GDfM) unifies current Design-for-Manufacturability (DfM), Manufacturing-for-Design (MfD), and Design-for-Yield (DfY), coupling all of the above-mentioned dimensions within a new space where their inter-dependence is revealed and exploited. Tightly coupled physical-electrical-mechanical-process modeling and simulation, will allow early detection of the impact of design choices at all levels. This creates a 4D knowledge continuum reminiscent of the ideas of General Relativity, ones extremely rich in consequences for the future of nanoelectronic design.

More information about ISSCC 2007 may be found at: http://www.isscc.org/isscc/.

Advances in Analogue Circuit Design Conference (AACD) Will Convene on 27-29 March 2007

16th Annual Workshop to Showcase European Expertise in Semiconductor Design Applications

Jan Craninckx, Chair, SSCS-Benelux, craincj@imec.be, Jan Sevenhans, SSCS Region 8 Representative, jan_sevenhans@amis.com, Jan Van der Spiegel, SSCS Chapters Chair, jan@seas.upenn.edu

The 16th annual AACD workshop will be held on 27 – 29 March, 2007 in the Hotel Thermae Palace at the beautiful beach resort of Oostende, Belgium. SSCS is a technical cosponsor of this conference.

The Thermae Palace, a unique seaside hotel in Art Deco style, is conveniently located within walking distance of the bustling Oostende city centre.

The three-day workshop will feature 18 excellent speakers on the following topics:

- Sensors, Actuators and Power Drivers for the Automotive and Industrial Environment (Tue 27 March)
- Very High Frequency Front Ends (Wed 28 March)
- Integrated PA's from Wire line to RF (Thu 29 March)

A panel discussion will be organized every evening on the topic of the day to ensure a lively interaction with the audience. The AACD technical program committee for 2007 consists of

- Herman Casier, AMI Semiconductor Fellow, Belgium
- Michiel Steyaert, Catholic University, Leuven
- Arthur Van Roermund, Eindhoven University of Technology.

Europe has expertise in a rich variety of semiconductor design applications: high-reliability and high-voltage automotive, medical for hearing aids and bio sensors, space radiation hard circuits and telecom mixed signal and multimedia, among others.

Each year, a European company takes the initiative to support the AACD local and logistic organization to give the technical program committee leaders a free hand to invite the best international speakers for this three-day summary of advances in analogue circuit

design. This year, the AACD local organisation is supported by the Communication High Voltage Product group of AMI Semiconductor in Belgium, represented by Jan Sevenhans PhD, IEEE fellow, and technically co-sponsored by IMEC, Leuven, Belgium in cooperation with the SSCS-Benelux chapter.

Willy Sansen (KU Leuven), Jan Huijsing (TU Delft) and Rudy Van de Plassche (Broadcom) started the AACD annual workshop in 1992 with the goal of bringing together analog circuit design experts in Europe. The proceedings with full paper contributions have been published each year summarizing the state of the art.

Over the past 15 years, the AACD workshop has covered timely topics such as biomedical circuits and sensors, telecom wireline copper and fiber optics, wireless public and LAN mixed signal systems on a chip, RF and baseband analogue radio circuits in bipolar and CMOS technologies, DSL drivers, A/D & D/A converters, low noise amplifiers, etc. It has taken place in Scheveningen, Leuven, Eindhoven, Villach, Lausanne, Como, Copenhagen, Nice, Munich, Noordwijk, Spa, Graz, Montreux, Limerick and Maastricht.

It will be our pleasure to welcome a large group of silicon circuit and technology engineers and researchers involved in analogue and RF IC design in automotive, telecom and all industrial and other applications for this 16th AACD!

More information may be found at www.aacd.ws/ and aacd2007@amis.com

From left, Jan Van der Spiegel, SSCS Chapters Chair (University of Pennsylvania), Jan Craninckx, SSCS-Benelux Chair (IMEC, Belgium), and Jan Sevenhans, SSCS Region 8 Representative (AMI Semiconductor).

From left, Dr. Van De Plassche, Dr. Sansen and Dr. Huijsing at the inaugural AACD conference in Scheveningen, The Netherlands, 1992.

Corcoran, Kornegay, H. S.Lee, T. Lee, and Van der Spiegel Elected to SSCS AdCom

John J. Corcoran

Kevin Kornegay

Hae-Seung (Harry) Lee

Thomas H. Lee

Jan Van der Spiegel

The SSCS membership re-elected five members to the Solid-State Circuits Society Administrative Committee (AdCom) for terms beginning 1 January, 2007.

Jan Van der Spiegel and Thomas H. Lee were elected for a second term, and Kevin Kornegay and Hae-Seung (Harry) Lee were elected as new members. The election also returned John J. Corcoran to the AdCom after a year off.

The AdCom includes fifteen members elected by the membership at large, with 5 members elected each year for a 3-year term. They meet twice a year, before the ISSCC in February and again in the summer.

The AdCom is responsible for overseeing Society technical activities, conferences and publications, and for initiating, developing and managing all Society activities. Stephen H. Lewis, SSCS past president and chair of the nominating committee, said that it recruited individuals with a broad understanding of the field and its working engineers.

Biographies of the 2007 AdCom members were published in the July Newsletter and are available on line. www.ieee.org/portal/pages/sscs/06July/AcCom_Candidates06.html

Design Council Newsletter Completes Inaugural Year

The year-old IEEE Council on Electronic Design Automation (CEDA) updates interested readers with its quarterly CEDA *Currents Newsletter*. SSCS is one of six founding member societies of the IEEE Council, which is best known for sponsoring the Design Automation Conference. In this first year of publishing CEDA *Currents Newsletter*, articles covered Logic Synthesis competition at IWLS, an interview with Robert Brayton, and opinion pieces on the state and need for formal verification.

The *Currents Newsletter* is available in two formats, on line at www.ieee-ceda.org, and as an embedded department within *IEEE Design & Test*, abridged and edited to conform to the publishing guidelines of that IEEE Computer Society magazine. The standalone version of the newsletter carries content additional to the D&T embedded coverage; a column related to interviews, opinions, counter-opinions and matters of general interest to the community. In addition, since the standalone version is published at a shorter schedule, it accommodates last minute listing of events and news. The standalone version is distributed online as well as in paper form at major CEDA events. The editors are Karti Mayaram (karti@eecs.oregonstate.edu) and Preeti Ranjan Panda (panda@cse.iitd.ac.in); Nanette Collins (nanette@nvc.com) also serves as support for IEEE CEDA's broader outreach activities.

In addition to *Currents Newsletter*, CEDA also publishes *IEEE Transactions on Computer Aided Design* which features in-depth technical articles for the researchers, and the *Design & Test magazine* which features technical articles that have direct impact on industrial practice.

Founding of CEDA

The Solid-State Circuits Society is a founding member of the IEEE Council on Electronic Design Automation (CEDA). The SSCSC AdCom voted its support in February 2005. Bryan Ackland and Jan Rabaey serve as SSCS Representatives on the new CEDA governing body whose President is Al Dunlop.

As a subject area, design automation has been spread across a number of technical activities within

the IEEE. These activities range from monolithic circuits to large information-processing systems. Within the context of electronic systems, computer-aided design (CAD) was synonymous with circuit simulation when it started as a discipline in the '60s. Now, CAD deals with a much broader set of concerns. Those issues continue to evolve with technological advances in materials, processing, devices, and circuits. Generally, they're put under the umbrella of electronic design automation (EDA).

On one side of the spectrum, the physical design of electronic circuits requires both deep knowledge and interaction with specialists on solid-state circuits and more broadly electronic devices. Yet the ubiquitous presence of programmable processor cores in integrated circuits has shifted much CAD work into the design of embedded software and hardware/software co-design--areas that are traditionally covered by computer scientists. By combining theory and practice, CAD is a key technology that boasts its own thriving industry. It also is a driver for the much larger semiconductor and electronic systems industry. It was natural for such an activity to have a diversified footprint within the IEEE as a technical organization. The range of CAD activities enabled the IEEE to benefit from the significant cross-fertilization of ideas from various mathematical and engineering optimizations and practices. As an organized activity, however, it was much harder for the organization to serve its members with information on interrelated advances and publications. The recognition of major advances was often secondary to major society activities.

CEDA was ratified by IEEE as a Technical Council effective January 2006. Within IEEE Technical Activities, a council like CEDA represents an organization with member societies. CEDA has six IEEE member societies: Antennas and Propagation; Circuits and Systems; Computer; Electron Devices; Microwave Theory and Techniques; and Solid-State Circuits. As with any IEEE technical activity, the ultimate goal is to advance the profession through a variety of technical activities from conferences and publications to standards. To serve members who are spread across various member societies, CEDA brings together several important resources. It provides conferences and publications to its technical community. As of this writing, the co-sponsored conferences include DAC, ICCAD, and Design and Test in Europe (DATE). CEDA enjoys special relationships with focused technical activities, such as DATC and TTTC in the Computer Society and CANDE within the Circuits and Systems Society. CEDA also is participating in the DARPA/MTO activities in building the roadmap for electronic systems

Rajesh K. Gupta, the Vice President of Publications for CEDA says, "Clearly, we're pleased to receive such broad support and community momentum toward building this new Council. We also are humbled by the challenges facing the community, which must match the pace of innovation by rapidly drawing new talent and entrepreneurship to the field. We need to engender technical activities that excite and challenge our audience and readership to new capabilities and opportunities. From this promising start, we hope to build years of exciting innovation and invention in electronic design automation."

IEEE Undergraduate Teaching Award

Nomination Deadline - January 31st

The IEEE Undergraduate Teaching Award is a Technical Field Award of the Institute established by the Board of Directors in 1990 to honor teachers of electrical and electronics engineering and the related disciplines, 'for inspirational teaching of undergraduate students in the fields of interest of the IEEE.'

A primary goal of the IEEE is to ensure that the Institute Awards Program provides due recognition for superior achievement in the engineering profession. To that end, and in response to the desire of the membership, the Awards Board, and Board of Directors that the field of education be more broadly recognized, this award for undergraduate teaching was added to the Awards Program.

Selection criteria include such contributions as curriculum development, authorship of course materials, involvement with students and faculty in advisory capacities, as well as 'attracting students to engineering and scientific professions, and preparing them for effective careers in engineering and the sciences.'

Recipient selection is administered by the IEEE Awards Board through the Technical Field Awards Council. It is presented to an individual only.

The award consists of a bronze medal, certificate and honorarium.

For a nomination form, list of past recipients and committee roster see:

www.ieee.org/awards/sums/ungrad.xml

IEEE Leon K. Kirchmayer Graduate Teaching Award

Nomination Deadline - 31 January

The IEEE Graduate Teaching Award is a Technical Field Award established by the Board of Directors in 1990 and renamed in honor of Leon K. Kirchmayer in 2002. Dr. Kirchmayer was well known and revered throughout the world for his commitment to students and education.

This award honors teachers of electrical and electronics engineering and the related disciplines, 'for inspirational teaching of graduate students in the IEEE fields of interest.'

A primary goal of the IEEE is to ensure that the Institute Awards Program provides due recognition for superior achievement in the engineering profession. To that end, and in response to the desire of the membership, the Awards Board, and Board of Directors that the field of education be more broadly recognized, this award for graduate teaching was added to the Awards Program. Selection criteria include such contributions as curriculum development, authorship of course materials, involvement with students and faculty in advisory capacities, as well as 'attracting students to engineering and scientific professions, and preparing them for effective careers in engineering and the sciences.'

Recipient selection is administered by the IEEE Awards Board through the Technical Field Awards Council. It is awarded to an individual only.

In the evaluation process, the following criteria are considered: excellence in teaching graduate students, curriculum development with the inclusion of current research and development knowledge that reflects the state of the art in courses, authorship of course material for graduate students; and involvement with and direction of students to prepare them for effective careers in engineering and the sciences, and the quality of the nomination.

The award consists of a bronze medal, certificate and honorarium.

For nomination form, list of past recipients and a committee roster:

www.ieee.org/awards/sums/gradtch.xml

Call for Nominations: SSCS Predoctoral Fellowships 2007 – 2008

Due Date is 1 May, 2007

Nominations for the Society's Predoctoral Fellowships in solid-state circuits are due on 1 May, 2007 for the academic year 2007-2008. The one-year awards will include a stipend of $15,000, tuition and fees up to a maximum of $8,000, and a grant of $2,000 to the department in which the recipient is registered. A maximum of two awards will be made.

Applicants must have completed at least one year of graduate study, be in a Ph.D. program in the area of solid-state circuits, and be a member of IEEE. The award will be made on the basis of academic record and promise, dissertation research program, and need.

Applications should be in electronic format and must include the following items:

A Short (one-page) Biography - including IEEE membership number.

Academic Records - including a copy of all relevant undergraduate and graduate transcripts.

Graduate Study Plans - including a summary of what has been completed and what is planned (about 2 pages is appropriate), plus a list of any publications authored or co-authored. A copy of each publication is desirable. Work that must be done to complete the graduate program of study should be explained -- why it is important, and what is novel about its approach -- as well as the importance of SSCS predoctoral fellowship support toward completion of the doctoral degree.

Letters of Recommendation - At least two letters of recommendation are required; one should be from the principal advisor. These letters should address academic record, accomplishments and promise, graduate study research program, and need.

Deadline: 1 May 2007

Please email your application materials to:

sscsFellowship@ieee.org.

Electronic file submission is preferred but if paper files are all you can provide, either fax them to +1 732-981-3401 or mail to:

IEEE-SSCS Executive Office
Predoctoral Fellowship
445 Hoes Lane
Piscataway, NJ 08854

SSCS EVENTS CALENDAR

Also posted on www.sscs.org/meetings

SSCS SPONSORED MEETINGS

2007 ISSCC International Solid-State Circuits Conference
www.isscc.org
11– 15 February 2006
San Francisco Marriott Hotel, San Francisco, CA, USA
Paper deadline: Passed
Contact: Courtesy Associates,
ISSCC@courtesyassoc.com

2007 Symposium on VLSI Circuits
www.vlsisymposium.org
14–16 June 2007
Kyoto, Japan
Paper deadline: 10 January 2007
Contact: Phyllis Mahoney,
vlsi@vlsisymposium.org
or Business Center for Academic Societies, Japan,
vlsisymp@bcasj.or.jp

2007 Custom Integrated Circuits Conference
http://www.ieee-cicc.org/
16–19 September 2007
San Jose, CA, USA
Paper deadline: TBD
Contact: Ms. Melissa Widerkehr
cicc@bis.com

2007 A-SSCC Asia Solid-State Circuits Conference
www.a-sscc.org/
12–14 November 2007
Seoul, Korea
Paper deadline: TBD
Contact: *ckwang@cc.ee.ntu.edu.tw*

SSCS PROVIDES TECHNICAL CO-SPONSORSHIP

2007 International Conference on VLSI Design
www.vlsiconference.com/
6–10 January 2007
Bangalore, India
Paper deadline: Passed
Contact: VLSI Secretariat:
sum_mahesh@yahoo.co.in

Advances in Analogue Circuit Design (AACD) Conference
www.aacd.ws/
27–29 March, 2007
Oostende, Belgium.
Paper deadline: TBD
Contact: *aacd2007@amis.com*

2007 Design, Automation and Test in Europe
www.date-conference.com/conference/next.htm
16–20 April, 2007
Acropolis, Nice, France
Paper deadline: Passed
Contact: *sue.menzies@ec.u-net.com*

2007 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)
vlsidat.itri.org.tw
25 Apr - 27 Apr 2007
Hsinchu, Taiwan
Paper Deadline: Passed
Contact: Ms. Stacey C.P. Hsieh
stacey@itri.org.tw

2007 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)
vlsidat.itri.org.tw
25 Apr - 27 Apr 2007
Hsinchu, Taiwan
Paper Deadline: Passed
Contact: Elodie J.F. Ho
elodieho@itri.org.tw

2007 Radio Frequency Integrated Circuits Symposium
www.rfic2007.org
3–8 June 2007
Honolulu, Hawaii
Paper deadline: 8 January 2007
Contact: Dr. Luciano Boglione
l.boglione@ieee.org

2007 Design Automation Conference
www.dac.com
4–8 June 2007
San Diego, CA, USA
Paper deadline: Passed
Contact: Kevin Lepine, Conference Manager
kevin@mpassociates.com

2007 IEEE Symposium on VLSI Circuits
www.vlsisymposium.org
14 Jun - 16 Jun 2007
Kyoto, Japan
Paper Deadline: 10 January 2007
Contact: Ms. Phyllis W. Mahoney
phyllism@widerkehr.com

ESSCIRC/ESSDERC 2007 - 37th European Solid State Circuits/Device Research Conferences
www.esscirc.org
11 Sep - 13 Sep 2007
Munich, Germany
Paper Deadline: 7 April 2007
Contact: Mr. Philip Teichmann
teichmann@tum.de

2007 IEEE Bipolar/BiCMOS Circuits and Technology
Meeting - BCTM
30 Sep - 02 Oct 2007
Boston Marriott Long Wharf, Boston, MA
Paper Deadline: TBD
Contact: Ms. Janice Jopke
ccs@mn.rr.com

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