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SMS QPSK/FDMA System Specification

eutelsat
communications via satellite

EESS 501 REVISION HISTORY

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1/0	14 November 1994	Original Issue
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1. INTRODUCTION

1.1. GENERAL

The scope of this document is to define the equipment characteristics of the SMS QPSK/FDMA System.

Mandatory requirements, i.e. requirements that have to be met by the SMS QPSK/FDMA equipment, are contained in the paragraphs marked by a vertical line in the left-hand margin, as shown for this paragraph.

The Eutelsat satellite multiservice system (SMS) is suitable for the transmission of the following services:

(a) data
(b) text and images
(c) voice

Specific applications for which the system is particularly suitable are as follows:

(i) videoconferencing
(ii) audioconferencing
(iii) computer-to-computer transfer
(iv) remote printing
(v) packet switched data carrier
(vi) fast facsimile
(vii) teletex
(viii) slow scan TV
(ix) electronic mail

This list is not exhaustive.

SMS carriers use coherent QPSK modulation and rate 3/4 or rate 1/2 convolutional coding with Viterbi decoding. The rate 3/4 is a "punctured" type of convolutional code and is constructed from a rate 1/2 encoder by periodically deleting specific bits from the rate 1/2 output bit sequence.

The present document specifies two FEC rates, rate 1/2 and rate 3/4. For rate 3/4 compliance with the following sections of the present document are optional: Section 2; Section 3.2.1; Section 3.2.2; Section 3.2.3.3; Section 5.2. Nevertheless, it is strongly recommended that these optional requirements be met for carriers using rate 3/4 FEC and with information rates lower than 2048 kbit/s.

Carriers in the Eutelsat SMS Open Network shall use equipment with the characteristics specified in the present document in conjunction with standard SMS earth stations. These standard earth stations are specified in EESS 500 (Satellite Multiservice System (SMS) Earth Station Standard - Standard S).

The earth stations used for reception of Rate 3/4 carriers in the Eutelsat SMS Open Network shall be of the SMS Standard S-1 or SMS Standard S-2 earth station type.

Due to the high power required with Rate 3/4 code in conjunction with a Standard S-3 receive earth station, this combination is not offered in the SMS Open Network.

Figure 1 illustrates the transmit and receive side channel unit.

The information bit stream is delivered at the input to the transmit channel unit, where, if multiplexed with other information bit streams (e.g. when interface H is provided) demultiplexing is performed. Then a synchronous frame structure is added to the information bit stream. The resulting bit stream is scrambled to provide energy dispersal. Forward Error Correction is employed before coherent quadrature phase shift keyed (QPSK) modulation is applied. The frequency at the output of the transmit channel unit is referred to as the intermediate frequency, IF. The signal is then upconverted to the radio frequency, RF, and amplified for transmission to the satellite.

The receive-side channel unit receives the IF signal from the output of the down converter. The signal is demodulated, decoded in the Viterbi decoder, de-scrambled and after removal of the overhead the information bit stream is delivered to the output in some cases after re-multiplexing (e.g. when interface H is provided).

1.2 QPSK/FDMA SYSTEM USING RATE 1/2 FEC

The QPSK/FDMA System offers an easy way of establishing digital data circuits in point-to-point and point-to-multipoint configurations.

The following customer bit rates can be provided:

(i) 2.4 kbit/s
(ii) 4.8 kbit/s
(iii) 9.6 kbit/s
(iv) 48 kbit/s
(v) n x 64 kbit/s where n = 1, 2, 4, 6, 12, 18, 24 and 30. (Other values of n in accordance with Table 1 could be provided at a later date if requested by customers).

In addition 2.048 Mbit/s will be available with restriction in the use of bits equivalent to time slot zero (TS0) of ITU-T G.704 Recommendation.

Figure 2 presents a typical access from the Customer to the earth station, showing the different interfaces in the path between the Customer Equipment and the earth station. Typical customer interface requirements are given in Table 1.

The information rate transmitted via the satellite ranges from 64 kbit/s to 1920 kbit/s and in the case of a 2048 kbit/s carrier is 1984 kbit/s if time slot 16 (TS16) of ITU-T G.704 Recommendation is used to transmit information.

1.3 QPSK/FDMA SYSTEM USING RATE 3/4 FEC

The carrier information bit rate shall be n x 64 kbit/s, with $1 \leq n \leq 120$.

An overhead of up to 12% may be added to the information bit rate of the carrier to permit the transmission of ITU-T R2 Signalling information, the provision of Engineering Service Circuits, the provision of synchronization and the provision of maintenance and alarm bits based on ITU-T M.20 Recommendation.

2 TERRESTRIAL INTERFACE

2.1 GENERAL

The provision of interface H is optional but the signal format and characteristics at the output of the transmit framing unit shall be as if interface H was provided.

2.2 INTERFACE H

2.2.1 Multiplex Structure

The recommended multiplex structure across interface H shall be as defined in the following tables, and shall conform to ITU-T G.704 Recommendation:

(a) Table 2 - 2.4, 4.8, 9.6 kbit/s
(b) Table 3 - 48 kbit/s
(c) Table 4 - 48 kbit/s (Point-to-point) associated with a ITU-T X.22 customer interface.
(d) Table 5 - n x 64 kbit/s

2.2.2 Electrical

All 2.048 Mbit/s signals shall conform to ITU-T G.703 Recommendation.

2.2.3 Timing

The timing of the digital signals at interface H in both directions of transmission shall be derived in one of three ways:

(i) from a national clock with an accuracy of 1 part in 10^{11} as recommended in ITU-T G.811 Recommendation.
(ii) from a local earth station clock with an accuracy of at least 1 in 10^{9} over any 40 day period.
(iii) from an incoming clock received from a remote earth station by satellite.

2.2.4 Jitter

The 64 kbit/s and 2048 kbit/s signals shall conform to ITU-T G.823 Recommendation.

3 CHANNEL UNIT CHARACTERISTICS

3.1 GENERAL

The channel unit consists of the following:

(1) framing unit

(2) encrypter/decrypter (optional)

(3) scrambler/descrambler

(4) FEC encoder/decoder

(5) modulator/demodulator

The channel unit shall utilize coherent QPSK modulation along with Rate 1/2 or Rate 3/4 FEC. The FEC shall be convolutional encoded with Viterbi decoding.

Figure 1 illustrates the transmit and receive side channel unit.

In the case of n x 64 kbit/s ($1 \leq n \leq 30$) user rate and Rate 1/2 FEC the channel unit demultiplexes and multiplexes the 2.048 Mbit/s channel and includes the signalling and alarm processing.

Plesiochronous buffering is included on the receive side.

The channel unit equipment is to be considered as a separate maintenance entity as defined in ITU-T M.20 Recommendation. This entity therefore supervises the continuity of the transmission and detects certain fault conditions.

3.2 FRAMING UNIT

3.2.1 Frame structure

3.2.1.1 General

A frame structure is defined in order to enable transmission of synchronization, signalling, monitoring and control information over the satellite link. This frame structure is optional for carriers using Rate 3/4 FEC.

The frame comprises 480 bits of customer data, an 8-bit alignment field (byte 0), an 8-bit message field (byte 32), and 16 bits for signalling (bytes 16 and 48). The structure is shown in Figure 3, which also indicates the content and bit allocation in the alignment and message fields.

3.2.1.2 Frame alignment

Frame alignment is carried out in the channel receiver using the frame alignment signal, comprising a 7-bit code in byte 0. Bit 2 in byte 32 is set to 1 in order to avoid simulation of the frame alignment signal.

Frame alignment will be assumed to be lost when three or four consecutive frame alignment signals have each been received with one or more errors.

Frame alignment will be assumed to have been recovered when the following sequence is detected:

- for the first time the presence of the correct frame alignment signal in byte 0,
- the absence of the frame alignment signal in byte 32 by verifying that bit 2 is a '1',
- for the second time the presence of the correct frame alignment signal in byte 0 of the next frame.

In the event of loss of alignment, continuous frame alignment signal search shall be initiated. On correct receipt of a frame alignment signal the recovery sequence given in the previous paragraph shall be initiated.

3.2.1.3 Multiframe

A 64-frame multiframe is defined, for the purpose of synchronization of the encryption and scrambling subsystems, and to carry channel identification and key identification codes.

The multiframe message is carried in bit 4 of byte 32 and comprises a 16-bit unique word and three 8-bit messages for station identification, channel identification and a spare. The initialization vector, and the key identification are carried in bits 7 and 8 of byte 32. The multiframe structure is shown in Figure 4.

The start of the multiframe will be generated in the frame following that in which the last bit of the multiframe unique word is received, and in each 64th frame thereafter. The unique word must be received with not more than one error.

The unique word window shall remain open continuously. If the unique word is received with more than one error in 16 consecutive multiframe periods the multiframe will be considered to be lost.

Multiframe alignment will be assumed to have been recovered when the first multiframe unique word is received with not more than one error.

The instant of the start of the multiframe is the first bit of byte 0 following the end of the multiframe unique word.

3.2.1.4 Allocation of Data Time Slots

The allocation of data time slots of interface H to the relevant bytes of interface K shall be as given in Tables 6 to 8 for values of n = 1, n = 2 and n = 4.

The frame structure at interface K is consistent with ITU-T G.704 Recommendation. Therefore no conversion is necessary in the case of a customer bit rate of 1920 kbit/s (n = 30).

For other values of n the same approach shall be adopted, following the rules below:

- The channel bit rate shall be

$$\frac{n \times 2048 \text{ kbit/s}}{30}$$

- The frame length shall be

$$\frac{30 \times 250\ \mu s}{n}$$

- Each frame shall start with byte 0 containing the frame alignment with the bit sequence: X001 1011 (see Table 6).
- After 15 bytes of customer data, byte 16 follows with signalling information defined in Section 3.2.2.
- After a further 15 bytes of customer data, byte 32 follows containing system management information with the bit sequence X1ae YYee (see Table 6).
- After a further 15 bytes of customer data, byte 48 follows with signalling information also defined in Section 3.2.2.
- After another 15 bytes of customer data, each frame ends with byte 63.
- The customer data at interface K are contained in 60 bytes with the following sequence: bytes 1 to 15, bytes 17 to 31, bytes 33 to 47 and bytes 49 to 63.
- These 60 data bytes shall be allocated to the data time slots which are arranged in a defined consecutive order at interface H. Byte 1 shall contain the information of the lowest designated data time slot of frame m at interface H, where m is the first 0.125 ms frame.

- After n bytes the information of the data time slots of frame m+1 follows, etc., until the 60 data bytes are filled and a new frame at interface K starts.

- Values of n which do not divide exactly into 60, require more than one frame to complete the sequence of data time slots of interface H. Therefore these values of n shall be restricted to n = 8, 16, 18 and 24. In these cases two, three or four frames are required to complete the sequence. The first frame in the sequence is defined as frame 0 in the multiframe (see Figure 4) and successive appropriate frames.

- In the special case of n = 18 the sequence can only be completed after three multiframes. For this purpose a three multiframe unit is defined in Section 3.2.2.2 regarding the special case of n = 18.

3.2.2 Transmission of Signalling Information

3.2.2.1 Message Content

If Interface H is used the transmitting channel unit shall transmit the signalling message contained in the relevant a, b, c and d signalling bits of time slot 16* at interface H (G.704).

The receiving channel unit shall transfer this signalling message to the relevant a, b, c and d signalling bits in time slot 16 of interface H.

The signalling bits sequence at interfaces H and K shall correspond exactly.

3.2.2.2 Message Structure

On the satellite path (interface K) the signalling message is carried in bytes 16 and 48 (see Figure 3).

The allocation of bits shall be as given in Tables 9 to 11 for values of n = 1, n = 2 and n = 4.

This message structure is consistent with ITU-T G.704 Recommendation. Therefore no conversion is necessary in the case of a customer bit rate of 1920 kbit/s (n = 30).

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* Note: For videoconference transmissions, time slot 16 at interface H can contain encoded video information instead of signalling bits..

For other values of n consistent with Section 3.2.1.4 the allocation shall follow the rules below:

- Byte 16 of frame 0 in the multiframe shall consist of the bit sequence: 0000 1011.
- Byte 48 of frame 0 and bytes 16 and 48 of frames 1 to 7, which together total 15 bytes, shall contain 30 sets of abcd bits of the relevant signalling channels in time slot 16, arranged in the same defined consecutive order as under 3.2.1.4. The first four bits of byte 48 of frame 0 shall be the set of abcd bits of the lowest designated relevant signalling channel of multiframe p at interface H, where p is any 2 ms multiframe.
- After n sets of abcd bits the information of the signalling channels of the multiframe p+1 follows, etc., until the 30 sets of abcd bits are filled.
- In the case of values of n which divide exactly into 30, the described procedure is repeated for frames 8 to 15, 16 to 23 etc., until the multiframe at interface K ends, with frame 63.
- In the case of values of n which divide exactly into 60, byte 16 of frame 8 shall consist of the bit sequence: 0000 0000, and the allocation of signalling channels shall continue as described before up to frame 15. The procedure is repeated for frames 16 to 31, 32 to 47 and 48 to 63.
- In the case of values of n which divide exactly into 120, bytes 16 of frames 8, 16 and 24 shall consist of the bit sequence: 0000 0000, and allocation of signalling channels shall continue as described before up to frame 31. The procedure is repeated for frames 32 to 63.
- In the case of n=16, which divides exactly into 240, bytes 16 of frames 8, 16, 24, 32, 40, 48 and 56 shall consist of the sequence: 0000 0000, and the allocation of signalling channels shall continue as described before up to the end of the multiframe.

- In the case of n = 18 three multiframes numbered 0, 1 and 2 shall be considered as a unit. Within this three multiframe unit the bytes 16

  of frames 0, 24 and 48 in multiframe 0,
  of frames 8, 32 and 56 in multiframe 1 and
  of frames 16, and 40 in multiframe 2 shall consist of the bit sequence 0000 1011

  The bytes 16 of all the other frames 0, 8, 16, 24, 32, 40, 48, and 56 within the three multiframe unit shall consist of the sequence: 0000 0000. The allocation of the signalling channels shall start with frame 0 of multiframe 0 and shall continue as described before up to the end of multiframe 2.

  The start of each three multiframe unit is defined as byte 0 of frame 0 following the multiframe unique word of multiframe 2 in which the bytes 16 in both frames 16 and 40 consist of the bit sequence 0000 1011.

In accordance with Section 3.2.1.4, signalling allocation for values of n which do not divide exactly into 240, except for n = 18, are not defined.

Table 12 summarizes the above by indicating those frames in which the contents of byte 16 does not consist of abcd bits.

3.2.3 Buffering Requirements

3.2.3.1 Delay Variation Due to Satellite Motion

It may be assumed that the maximum transmission delay variation due to the satellite motion will be 0.54 milliseconds for Eutelsat satellites.

These maximum variations refer to the peak-to-peak values and include both uplink and downlink contributions.

3.2.3.2 Buffer Capacity

The buffer capacity shall be at least 16 ms, except for the case in which the channel is in one direction, and has no associated return channel, when buffering is not required.

3.2.3.3 Slip Control

The buffer shall be reset whenever the channel suffers loss of service, and shall be reset when the buffer reaches saturation or becomes empty.

Any slip, including those caused by resetting the buffer, shall be a multiple of one frame period (as defined in Section 3.2.1.1) with an accuracy equal to that of the clock used to time the terrestrial side of the buffer.

With the buffer capacity as defined in Section 3.2.3.2 and the clock stability of Section 2.2.3, the resulting time interval between frame slips will be at least 40 days.

3.3 ENCRYPTION

3.3.1 General

The use of encryption on the satellite link is optional, and the encryption method is subject to bilateral agreement.

Bits have been made available for the encryption function in the frame structure (see Section 3.2).

Encryption (if employed) shall be applied to the satellite link part of individual channels, and shall not produce error extension. Bytes 0, 16, 32 and 48 of the frame structure shall remain unencrypted.

The overhead bytes are not encrypted because they contain repetitive bit patterns which could assist unwanted code deciphering were they encrypted.

3.3.2 Encryption Failure Detection

The fault condition FE2 (see Section 5) shall be indicated when failure of the encryption system occurs except when an alarm indication signal (AIS) is detected.

3.3.3 The Encryption System under AIS Condition

The encrypter shall provide an "all ones" condition if an "all ones" condition is received at the input. The decrypter shall provide an "all ones" condition if an "all ones" condition is received at the input. This condition shall be assumed to exist when all data bits of one frame are set to one.

Under these conditions, the encryption or decryption process shall not be bypassed but an independent AIS signal generator shall produce the "all ones" condition at the output of the cryptographic equipment.

3.4 SCRAMBLING

3.4.1 Rate 1/2 FEC

3.4.1.1 Principle

Synchronous scrambling shall be applied to all customer data, including encrypted data and the signalling channels (bytes 16 and 48). During the framing and message fields of the overhead structure (bytes 0 and 32) the scrambling sequence continues but the output is disabled leaving these bytes unscrambled.

3.4.1.2 Sequence

The scrambler/descrambler configuration is shown in the schematic diagram of Figure 5.

The polynomial is $1 + X^{-14} + X^{-15}$.

Loading of the sequence 001001001001001 shall be initiated at the start of each multiframe, whereby the right-most bit i.e. the "1" shall be located in shift register number 15 as shown in Figure 5.

3.4.2 Rate 3/4 FEC

A synchronous scrambling with the characteristics defined in Section 3.4.1.2 or a self-synchronizing scrambler as specified in Section 3.4.2.1 shall be provided.

3.4.2.1 Self-synchronizing Scrambler

The self-synchronizing scrambler shall have a logic diagram equivalent to that shown in Figure 6, and the descrambler shall have the impulse response shown in Figure 7. It should be noted that this is a self-synchronizing scrambler and that a single error in the received data stream can produce 3 errors over an interval of 20 bits. For this reason the FEC encoder shall follow the scrambler at the transmit channel unit. At the receive channel unit, the descrambler shall follow the decoder

3.5 FORWARD ERROR CORRECTION

3.5.1 General

The function of the data codecs is threefold: 1) to generate appropriate coding bits and to interface with the modulator, 2) to accept the demodulated signal and to recover correct code synchronization and correct carrier phase, and 3) in conjunction with the demodulator to make use of the code for reliable decisions about the transmitted sequence of data bits.

Either Rate 1/2 or Rate 3/4 convolutional encoding with a soft decision Viterbi (maximum likelihood) decoding shall be employed.

3.5.2 Encoder

3.5.2.1 Rate 1/2 FEC

The Rate 1/2 convolutional encoder as shown in the functional diagram of Figure 8a shall be employed.

The encoder consists of a binary differential encoder followed by a 7-stage shift register with the outputs of selected stages being added modulo-2 to form the Rate 1/2 encoded symbols. This means that the code has a memory of six which together with the incoming data bit forms a constraint length of 7. The code generator polynomials are 133 and 171 in octal notation. Since the code is transparent to 180° carrier phase ambiguities, the incoming data stream is differentially encoded before encoding by the Rate 1/2 convolutional encoder.

3.5.2.2 Rate 3/4 FEC

The Rate 3/4 convolutional encoder as shown in the functional diagram of Figure 8b shall be employed.

This is a "punctured" type of convolutional code and is constructed from a Rate 1/2 encoder by periodically deleting specific bits from the Rate 1/2 output bit sequence.

The encoder consists of a binary differential encoder followed by a 7-stage shift register with the outputs of selected stages being added modulo-2 to form the Rate 1/2 encoded symbols. This means that the code has a memory of six which together with the incoming data bit forms a constraint length of 7. The code generator polynomials of the Rate 1/2 code are 133 and 171 in octal notation. Since the code is transparent to 180° carrier phase ambiguities, the incoming data stream is differentially encoded before encoding by the Rate 1/2 convolutional encoder.

The Rate 3/4 code is constructed by periodically deleting two specified bits from among six bits contained in three consecutive blocks of the original Rate 1/2 code. The bit deletion is performed in the following manner:

(a) In the first block, both coded bits are transmitted;

(b) In the second block, the bit generated by generator polynomial 133 is transmitted and the bit generated by generator polynomial 171 is deleted;

(c) In the third block, the bit generated by generator polynomial 133 is deleted, and the bit generated by generator polynomial 171 is transmitted.

3.5.3 Decoder

3.5.3.1 Rate 1/2 FEC

The decoding shall be performed by a soft decision Viterbi (maximum likelihood) decoder having the following characteristics:

- The coding gain shall be compatible with the required Eb/No (see Section 4).
- Soft quantization shall be used with at least 8 levels, and a metric calculation and updating compatible with the required Eb/No.
- A total steady state decoder delay of no more than 200 data bits.
- Internal synchronization for 90° carrier phase ambiguity and, if necessary, code synchronization shall be provided.
- Steady state error performance shall be achieved within 500 data bits of decoder start-up.
- Binary differential decoding of the serial output data stream shall be provided.
- Indication of the rate of error correction may be provided. For operational reasons this feature is strongly recommended.

3.5.3.2 Rate 3/4 FEC

The decoding is performed by first re-constructing the Rate 1/2 coded data by inserting "erasure" bits into the received data stream at the positions in which the original Rate 1/2 coded bits were deleted on the transmitting side. The re-constructed Rate 1/2 coded data is then decoded by a soft-decision Viterbi (maximum likelihood) decoder.

The decoder shall have the following characteristics :

- The coding gain shall be compatible with the required Eb/No. For this type of decoder 3 bit (8 level) quantization may be required as an input, and hence the demodulator would provide such an interface.
- Internal resolution for 90° carrier phase ambiguity and code synchronization shall be provided.
- Binary differential decoding of the serial output data stream shall be provided.
- It is recommended that an indication of the rate of error correction be provided for monitoring the performance of the carrier.

3.6 MODULATOR

For reference purposes, it is assumed that the modulator accepts two parallel data streams from the FEC encoder, designated the P channel and the Q channel.

3.6.1 Input Clock Jitter

The sinusoidal peak-to-peak jitter of the clock at the modulator input shall not exceed the mask of Figure 9 where M is a factor, dependent on the carrier bit rate according to the following:

M = 1 for 64 kbit/s and 128 kbit/s;
M = 2 for 256 kbit/s and
M = 8 for 1920 kbit/s.

3.6.2 Output Characteristics

The relationship between the bits to be transmitted and the carrier phase of the modulator output is given below:

Transmitted Bits		
P Channel	Q Channel	Resultant Phase
1	1	0°
0	1	+ 90°
0	0	+ 180°
1	0	+ 270° (-90°)

The phase accuracy at the modulator output shall be ±2°. The amplitude accuracy at the modulator output shall be ±0.2 dB.

The above specification has been written in terms of absolute phase encoding rather than differential encoding because carrier phase ambiguities are resolved by means of the FEC coding.

The output frequency of the modulator is designated as the IF frequency. The nominal centre of the IF frequency band is usually either 70 MHz or 140 MHz.

The output frequency of the modulator shall be adjustable with a frequency step of 22.5 kHz or a sub multiple of 22.5 kHz.

3.6.3 Modulator Spectrum Output

The transmitted Intermediate Frequency (IF) spectrum within the frequency range ±0.35 R Hz from the nominal centre frequency shall be equivalent to a spectrum present at the output of a filter following an ideal modulator, under the following conditions:

(a) The input to the QPSK ideal modulator is a R bit/s non-return-to-zero (NRZ) random sequence (with equal probability of 0 or 1);

(b) The filter has amplitude characteristics given in Figure 10;

(c) The filter has group delay characteristics given in Figure 11 or a phase response with less than ±4 degrees departure from a linear phase shift over the frequency range ±0.25 R about the nominal centre frequency.

Within the bandwidth 0.35 R to 0.75 R Hz away from the nominal centre frequency the envelope of the transmitted IF spectrum shall not exceed that obtained at the output of a filter following an ideal modulator, under the conditions given in (a), (b), and (c) above.

Outside the bandwidth ±0.75 R Hz from the nominal centre frequency the transmitted IF spectral density shall be at least 40 dB below the peak spectral density, measured in a 4 kHz band.

Over the frequency range ±0.35 R Hz from the nominal centre frequency (b) and (c) above are met by a filter consisting of the cascade of a group delay equalized 6 pole Butterworth filter (BT_s = 1.0) and sinc $^{-1}$ compensation (the overall BT_s of cascaded elements is equal to 1.5),

where:

$\text{sinc}^{-1} = \pi\Delta fTs/\sin(\pi\Delta fTs)$

and:

B = 3 dB double sided bandwidth of filter

Ts = Symbol period = 2/R baud

Δf = Displacement from centre frequency

R = Transmission rate in bit per second.

It should be noted that the transmitted IF spectrum requirement is mandatory, not the modulator filter response.

A mask of the power spectral density which will result from a modulator meeting the amplitude characteristics outlined above, is shown in Figure 12.

3.7 DEMODULATOR

A coherent QPSK demodulator shall be used. Bit timing shall be recovered and presented to the FEC decoder. The demodulator shall provide an output which is compatible with the soft decision decoder.

3.7.1 Demodulator Filter Characteristics

For the development of BER requirements the amplitude characteristics for the demodulator receive filter have been assumed as given in Figure 13. The group delay characteristics have been assumed as given in Figure 11.

The demodulator receive filter characteristics are nominally equivalent to a group delay equalized 6 pole Butterworth filter ($BT_s = 1.0$).

4 SYSTEM PERFORMANCE

4.1 GENERAL

The performance requirements of Section 4.3 shall be met under the operating conditions given in Section 4.2.

4.2 OPERATING CONDITIONS

4.2.1 Level Variations

The signal level of any channel at the receiver RF subsystem input may vary dynamically over the range of 14 dB.

4.2.2 Frequency Separation and Adjacent Carrier Levels

The nominal frequency separation between carriers of the same transmission bit rate is either n x 90 kHz for Rate 1/2 FEC or n x 60 kHz for Rate 3/4 FEC, where n x 64 kbit/s is the customer data rate (e.g. for n = 6 the customer data rate is 384 kbit/s and the nominal frequency separation between two equal carriers is either 540 kHz for Rate 1/2 FEC carriers or 360 kHz for Rate 3/4 FEC carriers). The level of an adjacent carrier of the same transmission bit rate shall be taken as 7 dB higher than the desired carrier level.

4.2.3 Phase Noise

4.2.3.1 Earth Stations

The phase noise induced on any transmitted carrier will satisfy either of the following two limits:

- Limit 1 The single sideband phase noise is assumed to consist of a continuous component and a spurious component. The single sideband power spectral density of the continuous component will not exceed the envelope shown in Figure 14.

  The largest single spurious component will not exceed -30 dB relative to the level of the transmitted carrier. The single sideband sum (added on a power basis) of all other individual spurious components will not exceed -36 dB relative to the level of the transmitted carrier. (The total phase noise including both sidebands can be up to 3 dB higher), or

- Limit 2 The single sideband phase noise due to both the continuous and spurious components integrated over the bandwidth 10 Hz to S Hz away from the centre frequency, where S is the symbol rate, will not exceed 2.0 degrees rms. (The total phase noise due to both sidebands shall not exceed 2.8 degrees rms.)

The phase noise requirement for the receive side is not specified but should be consistent with the carrier recovery system of the demodulator. As a minimum it is expected that the phase noise given above for the transmit side will be also met on the receive.

4.2.3.2 Satellite

The phase noise contributed by the satellite frequency translation is shown in Figure 15.

4.3 SYSTEM PERFORMANCE REQUIREMENTS

4.3.1 Modem Performance

When the modem is connected back-to-back at IF, through an additive white Gaussian noise channel and in the presence of two adjacent carriers of the same transmission rate under the conditions given in Section 4.2.2, the bit error ratio (BER) of the data channel measured on the terrestrial side of the FEC decoder after descrambling as a function of the energy per data bit (the data rate is the information rate plus overhead rate entering the FEC encoder) to noise density ratio (Eb/No) shall not exceed the values shown in Table 13.

The data pattern to be used for this test shall consist of a pseudo random sequence.

The BER performance shall include the effects of carrier and bit timing slips.

4.3.2 Bit Slip for Rate 1/2 FEC

The bit slip performance shall be better than one slip per 24 hours when the Eb/No at the demodulator input is 6.1 dB.

4.3.3 Recovery for Rate 1/2 FEC

4.3.3.1 General

After a complete break in the received signal, the following recovery requirements shall be met.

4.3.3.2 Carrier and Clock Recovery

When providing continuous mode data the demodulator shall recover carrier and clock in less than 32000 bits, assuming zero frequency offset and an Eb/No of 6.1 dB.

4.3.3.3 Decoder Recovery

The decoder shall provide the steady state performance as given in Section 4.3.1 within 500 bits of receiving the clock from the demodulator.

5 MAINTENANCE ALARM CONCEPT

5.1 GENERAL

The basis for this maintenance alarm concept is ITU-T M.20 Recommendation.

The channel unit maintenance entity is defined as the digital equipment between the interfaces H and K (see Figure 1).

Although the Eutelsat SCPC Satellite Multiservice System supports services of different bit rates, the recommended interface H complies with ITU-T G.704 Recommendation. Several channels of bit rates lower than 1920 kbit/s (minimum: 64 kbit/s) may be routed via interface H.

At interface K each channel is separate with its own digital structure. This structure contains not only the customer channel but also bytes for framing and signalling.

The fact that the signal is subject to FEC and scrambling is not to be considered with respect to the maintenance alarm concept.

5.2 FAULT CONDITIONS AND CONSEQUENT ACTIONS

Table 14 shows which consequent actions have to be taken after detection of specific fault conditions.

The channel unit shall detect the following fault conditions:

In the equipment

FE1 failure of power supply

FE2 failure of channel equipment

FE3 failure of common equipment.

From the terrestrial side across interface H

FH1 loss of incoming signal

FH2 loss of frame alignment

FH3 loss of multiframe alignment

FH4 BER 1 in 10^3 exceeded

FH5 alarm indication received from own terrestrial link, either in bit 3 of TS 0 not containing frame alignment signal or in bit 6 of TS 16 frame 0.

From the satellite across interface K

FK1 loss of incoming signal

FK2 loss of frame alignment (in byte 0)

FK3 loss of multiframe unique word (in bit 4 of byte 32)

FK4 BER of 1 in 10^3 exceeded. Measured on the frame alignment signal over any 1 minute period.

FK5 alarm indication received from remote earth station (in bit 3 of byte 32).

Further, with the detection of a fault condition, appropriate action shall be taken as follows:

AE prompt maintenance alarm generated.

AH1 AIS applied across interface H to indicate that a fault has been detected, and to be used as service alarm at own end. This AIS is transmitted as an "all ones condition" of the 2.048 Mbit/s signal across interface H.

AH2 alarm indication across interface H to be used as service alarm at own end. This is transmitted as state 1 in bit 3 of TS 0 not containing frame alignment signal.

AH3 AIS applied across interface H in relevant data time slots to indicate that a fault has been detected, and to be used as service alarm at own end. This AIS is transmitted as an "all ones condition" in the data time slots concerned.

AH4 channel individual alarm indication across interface H to be used as service alarm at own end. It is to be transmitted as "1111" condition of the relevant "abcd" signalling bits.

AH5 channel individual alarm indication across interface H to be used as service alarm at own end. It is to be transmitted as "b = 1" in the relevant signalling bits "abcd".

AH6 alarm indication concerning time slot 16 (TS 16) across interface H to be used as service alarm at own end. It is to be transmitted as state 1 in bit 6 of TS 16 frame 0.

AK1 AIS applied across interface K to indicate that a fault has been detected and to be used as service alarm at the distant end. This AIS is sent as an all 1's condition in all the bytes except bytes 0 and 32.

AK2 alarm indication to the remote earth station to be used as a service alarm at the distant end. It is to be transmitted as state 1 in bit 3 of byte 32.

AK3 channel individual alarm indication across interface K to be used as service alarm at the distant end. It is to be transmitted as "1111" condition of the relevant signalling bits "abcd".

	Bit rates at interface	ITU-T	Interface A		Remarks
			Functional Characteristics	Electrical Characteristics	
1	2400 bit/s	Note 1 X 21 bis X 21 V 26	V 24 V 24 X 24 V 24	V 28 V 28 X 27 V 28	
2	4800 bit/s	Note 1 X 21 bis X 21 V 27	V 24 V 24 X 24 V 24	V 28 V 28 X 27 V 28	
3	9600 bit/s	Note 1 X 21 bis X 21 V 29	V 24 V 24 X 24 V 24	V 28 V 28 X 27 V 28	
4	48 kbit/s	V 35 X 21 bis X 22 X 21 V36	V 35 V 35 X 24 X 24 V 24	V 35 V 35 X 27 X 27 V 10 and V 11	
5	64 kbit/s	X 21 V 35 V 36 X 50 Note 2	V 24 V 35 V 24	X 27 V 35 V 10 and V 11 G 703	
6	N x 64 kbit/s	X 21 V 35 V 36	X 24 V 35 V 24	X 27 V 35 V 10 and V 11	Possible values of n = 2, 3, 4, 5, 6, 8, 10, 12, 15, 16, 18, 20, 24 and 30 although n = 2, 4, 6, 12, 18, 24, and 30 will be offered initially.
7	2.048 Mbit/s Note 2	G 704 G 704		G 703 G 704	TSO is not transparent to the user. Video conference service.

Note 1: Baseband modem using interchange circuits 101 to 109, 113, 114, 115 and 142.
Note 2: Only available at interface (B).

TABLE 1: Customer Interface Requirements

BIT RATE AT INTERFACE (A)	MULTIPLEXING STRUCTURE AT INTERFACE (H)	SIGNALLING AND OPERATION ASPECTS
2.4 kbit/s 4.8 kbit/s 9.6 kbit/s	Should have a balanced X.50 multiplex structure in Tx and Rx. Either a 2.048 Mbit/s bearer with time slots in X.50 multiplex structure, or exceptionally separate 64 kbit/s channels in X.50 multiplex structure. The 64 kbit/s interface may conform to the codirectional interface as defined in ITU-T G.703 Recommendation. Generally single destination for each 64 kbit/s channel, although point-to-multipoint is possible.	Status bits are transmitted between (H) interfaces without processing. With network failure all bits in the 64 kbit/s channel are set to "1" including the framing bits. Only on a full time leased line basis.

Table 2: Multiplex Structure at Interface H

for 2.4, 4.8 and 9.6 kbit/s.

BIT RATE AT INTERFACE (A)	MULTIPLEXING STRUCTURE AT INTERFACE (H)	SIGNALLING AND OPERATION ASPECTS
48 kbit/s	Balanced X.50 bis multiplex structure. Either on a 2 Mbit/s bearer using any time slot except TSO and TS16, or exceptionally separate 64 kbit/s channels in X.50 bis multiplex structure. The 64 kbit/s interface may conform to the codirectional interface as defined in ITU-T G.703 Recommendation.	Status bits are transmitted between (H) interfaces without processing. For full time leased line operation no signalling channel is required. For network failure all bits in the 64 kbit/s channel shall be set to "1".

Table 3: Multiplex Structure at Interface H for 48 kbit/s.

BIT RATE AT INTERFACE (A)	MULTIPLEXING STRUCTURE AT INTERFACE (H)	SIGNALLING AND OPERATION ASPECTS
48 kbit/s (X.22)	Balanced X.50 multiplex structure. Either a 2 Mbit/s bearer with time slot in X.50 multiplex structure, or separate 64 kbit/s channel in X.50 multiplex structure. The 64 kbit/s interface may conform to the codirectional interface as defined in ITU-T G.703 Recommendation. Single destination for each 64 kbit/s channel.	Status bits are transmitted between (H) interfaces without processing. For network failure all bits in the 64 kbit/s channel are set to "1".

Table 4: Multiplex Structure at Interface H for 48 kbit/s with X.22 interface (Point-to-Point Only).

BIT RATE AT INTERFACE (A)	MULTIPLEXING STRUCTURE AT INTERFACE (H)	SIGNALLING AND OPERATION ASPECTS
n x 64 kbit/s	On one 2048 kbit/s bearer time slots need not be contiguous. One bearer can carry several n x 64 kbit/s channels. Outgoing and incoming channels shall be on the same time slots of the 2 Mbit/s bearer in the case of point-to-point. For a time slot on a bearer the order TS1, TS2... TSn in each frame across (H) towards (K) must be preserved at the corresponding remote interface (H) towards (G).	Network failure: All bits set to "1" in relevant time slots. Status bits are transmitted in TS 16.

Table 5: Multiplex Structure at Interface H for n x 64 kbit/s.

Interface H (G.704)		Interface K (Figure 3)	
frame	time slot	byte	sequence
---	---	0	X001 1011
1	m**	1	data of TS m
2	m	2	data of TS m
3	m	3	data of TS m
.	.	.	.
.	.	.	.
.	.	.	.
15	m	15	data of TS m
---	---	16	signalling*
16	m	17	data of TS m
17	m	18	data of TS m
.	.	.	.
.	.	.	.
.	.	.	.
30	m	31	data of TS m
---	---	32	X1 ae YYee***
31	m	33	data of TS m
.	.	.	.
.	.	.	.
.	.	.	.
45	m	47	data of TS m
---	---	48	signalling*
46	m	49	data of TS m
47	m	50	data of TS m
.	.	.	.
.	.	.	.
.	.	.	.
59	m	62	data of TS m
60	m	63	data of TS m
60 frames of .125 ms = 7.5 ms =======		One frame of 64 bytes = 7.5 ms =======	

Table 6: Allocation of data time slots for customer rate 64 kbit/s (n=1)

---

*) Signalling : (see Section 3.2.2)

**) "m" stands for any specific time slot of the PCM frame

***) "a" stands for the bit indicating backward alarm to remote end.
"e"stands for the bits concerning encryption messages
"X" = 1 if not used for other purposes
"Y" = 1 if not used for conferencing purposes (see Figure 3).

Interface H (G.704)		Interface K (Figure 3)	
frame	time slot	byte	sequence
---	---	0	X001 1011
1	m**	1	data of TS m
1	n**	2	data of TS n
2	m	3	data of TS m
.	.	.	.
.	.	.	.
.	.	.	.
8	m	15	data of TS m
---	---	16	signalling*
8	n	17	data of TS n
9	m	18	data of TS m
.	.	.	.
.	.	.	.
.	.	.	.
15	n	31	data of TS n
---	---	32	X1 ae YYee***
16	m	33	data of TS m
.	.	.	.
.	.	.	.
.	.	.	.
23	m	47	data of TS m
---	---	48	signalling*
23	n	49	data of TS n
.	.	.	.
.	.	.	.
.	.	.	.
29	n	61	data of TS n
30	m	62	data of TS m
30	n	63	data of TS n
30 frames of .125 ms = 3.75 ms =======		One frame of 64 bytes = 3.75 ms =======	

Table 7: Allocation of data time slots for customer rate 128 kbit/s (n=2)

---

*) Signalling : (see Section 3.2.2)
**) "m" and "n" stands for any specific time slot of the PCM frame
***) "a" = bit indicating backward alarm to remote end.
"e" = bits concerning encryption messages
"X" = 1 if not used for other purposes
"Y" = 1 if not used for conferencing purposes (see Figure 3).

Interface H (G.704)		Interface K (Figure 3)	
frame	time slot	byte	sequence
---	---	0	X001 1011
1	p**	1	data of TS p
1	q**	2	data of TS q
1	r**	3	data of TS r
1	s**	4	data of TS s
2	p	5	data of TS p
2	q	6	data of TS q
.	.	.	.
.	.	.	.
.	.	.	.
4	q	14	data of TS q
4	r	15	data of TS r
---	---	16	signalling*
4	s	17	data of TS s
5	p	18	data of TS p
.	.	.	.
.	.	.	.
.	.	.	.
8	q	31	data of TS q
---	---	32	X1 ae YYee***
8	r	33	data of TS r
.	.	.	.
.	.	.	.
.	.	.	.
12	p	47	data of TS p
---	---	48	signalling*
12	q	49	data of TS q
.	.	.	.
.	.	.	.
.	.	.	.
15	p	60	data of TS p
15	q	61	data of TS q
15	r	62	data of TS r
15	s	63	data of TS s
15 frames of .125 ms = 1.875 ms ========		One frame of 64 bytes = 1.875 ms ========	

Table 8: Allocation of data time slots for customer rate 256 kbit/s (n=4)

---

*) Signalling : (see Section 3.2.2)
**) "p", "q", "r", "s" = specific time slot of the frame
***) "a" = bit indicating backward alarm to remote end.
"e" = bits concerning encryption messages
"X" = 1 if not used for other purposes
"Y" = 1 if not used for conferencing purposes (see Figure 3

Interface H (G.704)		Interface K (Figure 3)		
abcd bits of signalling channel n in time slot 16		Frame	Byte	Sequence
Multiframe	Signalling channel No			
---	---	0 8•••56	16	0000 1011
1, 2	n, n	0 8•••56	48	abcd abcd
3, 4	n, n	1 9•••57	16	abcd abcd
5, 6	n, n	1 9•••57	48	abcd abcd
•	•	• • •	•	•
15, 1	•	• • •	•	•
•	•	• • •	•	•
•	•	• • •	•	•
•	•	• • •	•	•
12, 13	n, n	7 15•••63	16	abcd abcd
14, 15	n, n	7 15•••63	48	abcd abcd
abcd bits are sent every 2 ms.		abcd bits are sent 30 times in eight frames of 7.5 ms. $\frac{8 \times 7.5\text{ms}}{30}$ = 2 ms.		

Table 9: Allocation of Signalling Bits for Customer Rate 64 kbit/s (n=1).

Interface H (G.704)		Interface K (Figure 3)		
abcd bits of signalling channel n1 to n2 in time slot 16		Frame	Byte	Sequence
Multiframe	Signalling channel No			
---	---	0 8•••56	16	0000 1011
1	n1, n2	0 8•••56	48	abcd abcd (n1) (n2)
2	n1, n2	1 9•••57	16	abcd abcd (n1) (n2)
3	n1, n2	1 9•••57	48	abcd abcd (n1) (n2)
•	•	• • •	•	•
•	•	• • •	•	•
•	•	• • •	•	•
14	n1, n2	7 15•••63	16	abcd abcd (n1) (n2)
15	n1, n2	7 15•••63	48	abcd abcd (n1) (n2)
abcd bits are sent every 2 ms.		abcd bits are sent 15 times in eight frames of 3.75 ms. $\frac{8 \times 3.75 ms}{15}$ = 2 ms.		

Table 10: Allocation of Signalling Bits for Customer Rate 128 kbit/s (n=2).

Interface H (G.704)		Interface K (Figure 3)		
abcd bits of signalling channel n1 to n4 in time slot 16		Frame	Byte	Sequence
Multiframe	Signalling channel No			
---	---	0 16 32 48	16	0000 1011
1	n1, n2	0 16 32 48	48	abcd abcd (n1) (n2)
1	n3, n4	1 17 33 49	16	abcd abcd (n3) (n4)
2	n1, n2	1 17 33 49	48	abcd abcd (n1) (n2)
2	n3, n4	2 18 34 50	16	abcd abcd (n3) (n4)
•	•	• • •	•	•
•	•	• • •	•	•
•	•	• • •	•	•
7	n3, n4	7 23 39 55	16	abcd abcd (n3) (n4)
8	n1, n2	7 23 39 55	48	abcd abcd (n1) (n2)
---	---	8 24 40 56	16	0000 0000*
8	n3, n4	8 24 40 56	48	abcd abcd (n3) (n4)
•	•	• • •	•	•
•	•	• • •	•	•
•	•	• • •	•	•
14	n1, n2	1 30 46 62 4	48	abcd abcd (n3) (n4)
15		1 31 47 63 5	16	abcd abcd (n1) (n2)
15		1 31 47 63 5	48	abcd abcd (n3) (n4)
abcd bits are sent every 2 ms.		abcd bits are sent 15 times in 16 frames of 1.875 ms. $\frac{16 \text{ x } 1.875 \text{ ms}}{15}$ = 2 ms.		

Table 11: Allocation of Signalling Bits for Customer Rate 256 kbit/s (n=4)

* Note : Byte 16 of frame 8 etc. is a pure dummy byte to keep synchronism with interface H

		Contents of byte 16	
		0000 1011	0000 0000
	SMS Multiframe	Frames	Frames
$\frac{30}{n}$ = integer e.g. n = 1, 2, 6, 30	0	0 8 16 24 32 40 48 56	/
$\frac{60}{n}$ = integer e.g. n = 4, 12	0	0 16 32 48	8 24 40 56
$\frac{120}{n}$ = integer e.g. n = 8, 24	0	0 32	8 16 24 40 48 56
$\frac{240}{n}$ = integer e.g. n = 16	0	0	8 16 24 32 40 48 56
n = 18	0 1 2	0 24 48 8 32 56 16 40	8 16 32 40 56 0 16 24 40 48 0 8 24 32 48 56

Table 12 Contents of Byte 16 for Different Values of n.

	Eb/No in dB	
	FEC Rate	
BER	1/2	3/4
10^{-3}	4.2	5.3
10^{-4}	4.7	6.2
10^{-5}	5.4	7.0
10^{-6}	6.1	7.6
10^{-7}	6.7	8.3
10^{-8}	7.2	8.8
10^{-10}	9.0	10.3

Table 13: Modem Performance in IF back-to-back loop.

Consequent Actions / Fault Condition	AE	AH1	AH2	AH3	AH4	AH5	AH6	AK1	AK2	AK3
FE1	yes	yes (1)						yes (1)		
FE2	yes			yes (1)	yes (1)			yes (1)		
FE3	yes	yes (1)						yes (1)		
FH1	yes		yes					yes		
FH2	yes (2)		yes					yes		
FH3(5)	yes (2)						yes			yes
FH4	yes		yes					yes		
FH5									yes	
FK1	yes			yes	yes				yes	
FK2	yes (2)			yes	yes				yes	
FK3	yes			yes	yes				yes	
FK4	yes			yes	yes				yes	
FK5(4)					yes (3)	yes (3)				

Table 14: Fault Conditions and Consequent Actions of the Channel Unit Maintenance Entity

yes = action to be taken

(1) if practicable

(2) inhibited if AIS is received

(3) in the case of telephony, the blocking signal of the appropriate signalling system should be provided.

(4) this fault condition shall not be considered in the case of n = 30 (1920 kbit/s). In this case AH2 shall be passed on across interface H.

(5) this fault condition is not to be considered in the case of n = 30 (1920 kbit/s) or n = 31 (videoconferencing).

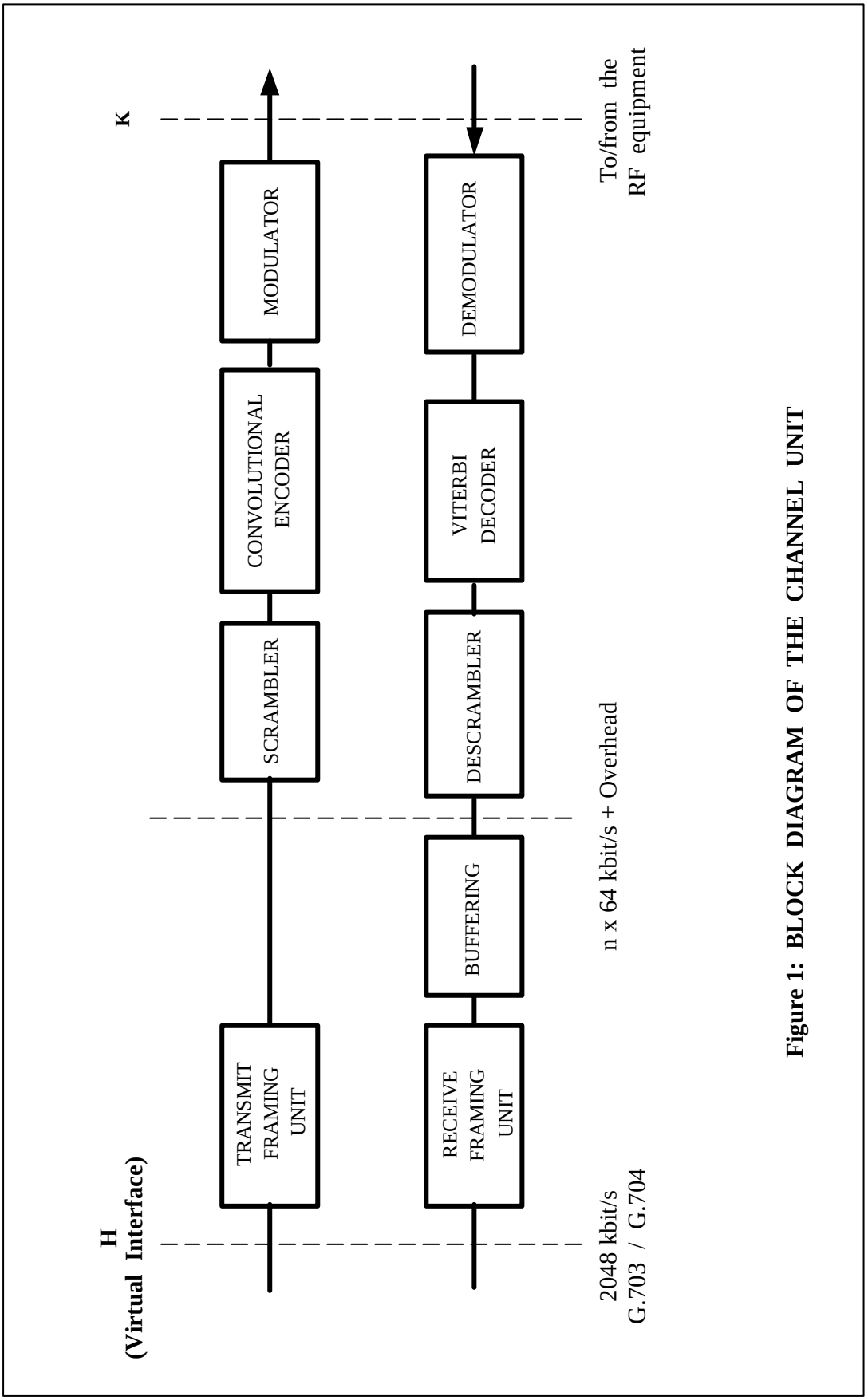


Figure 1: BLOCK DIAGRAM OF THE CHANNEL UNIT

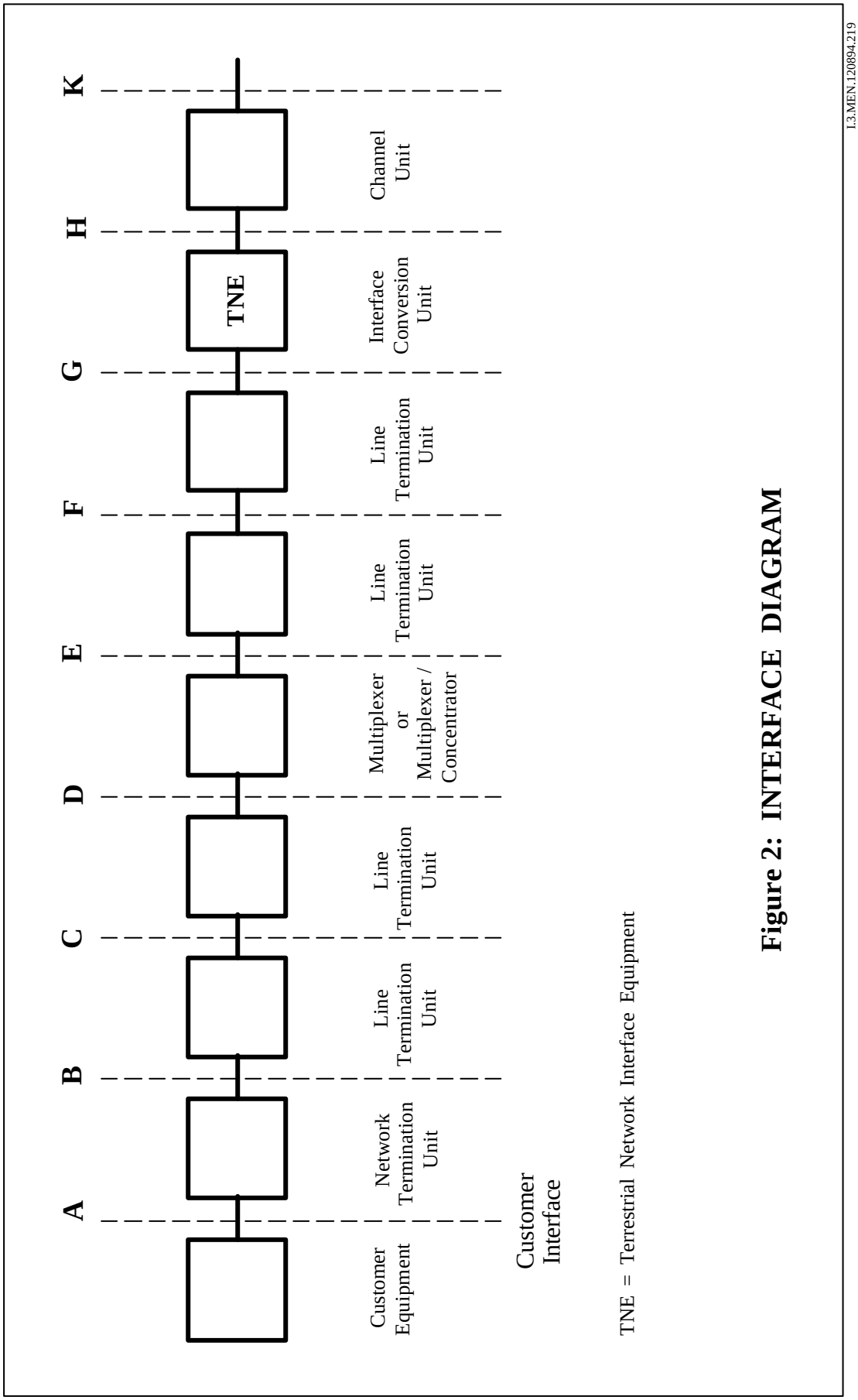


Figure 2: INTERFACE DIAGRAM

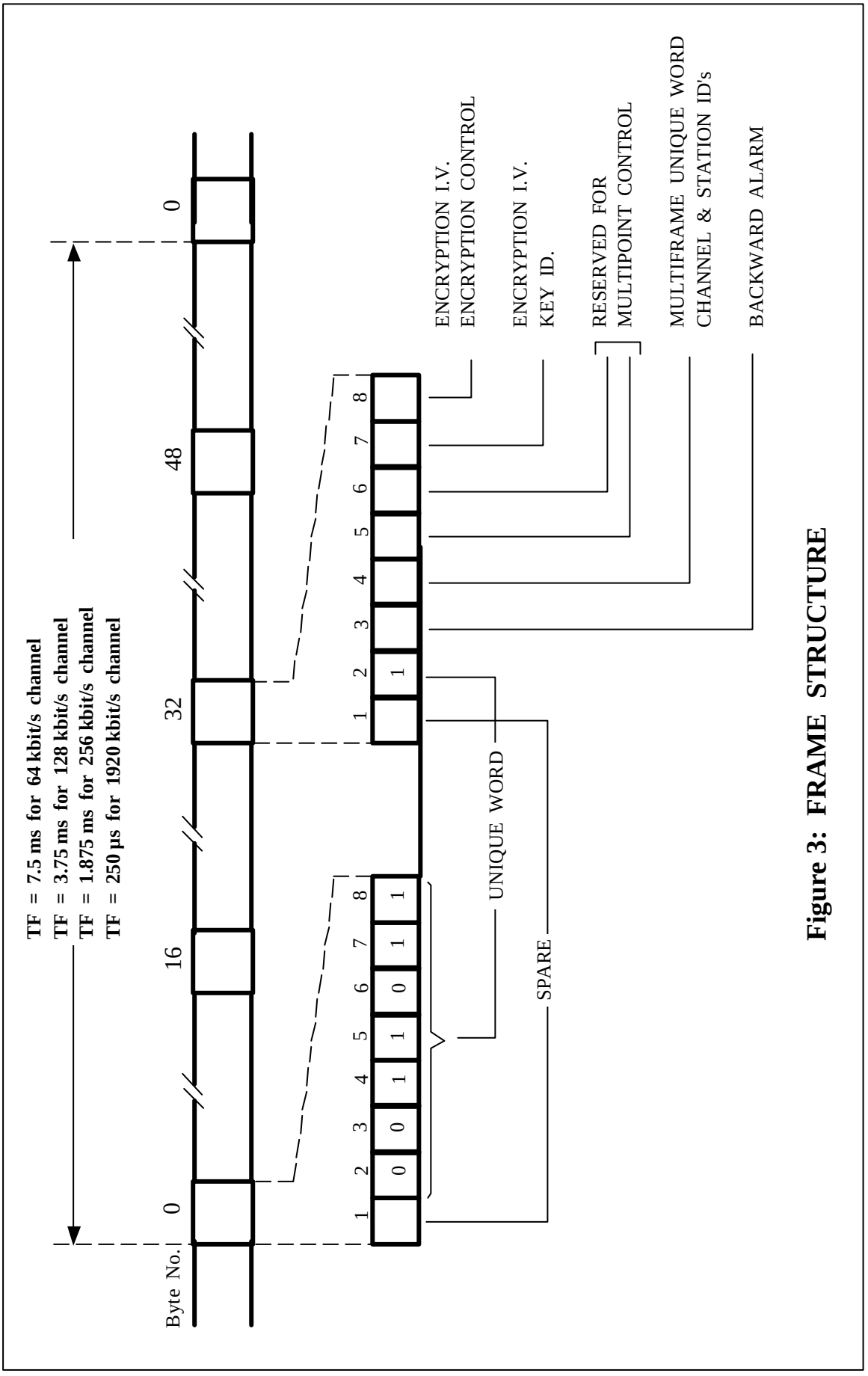


Figure 3: FRAME STRUCTURE

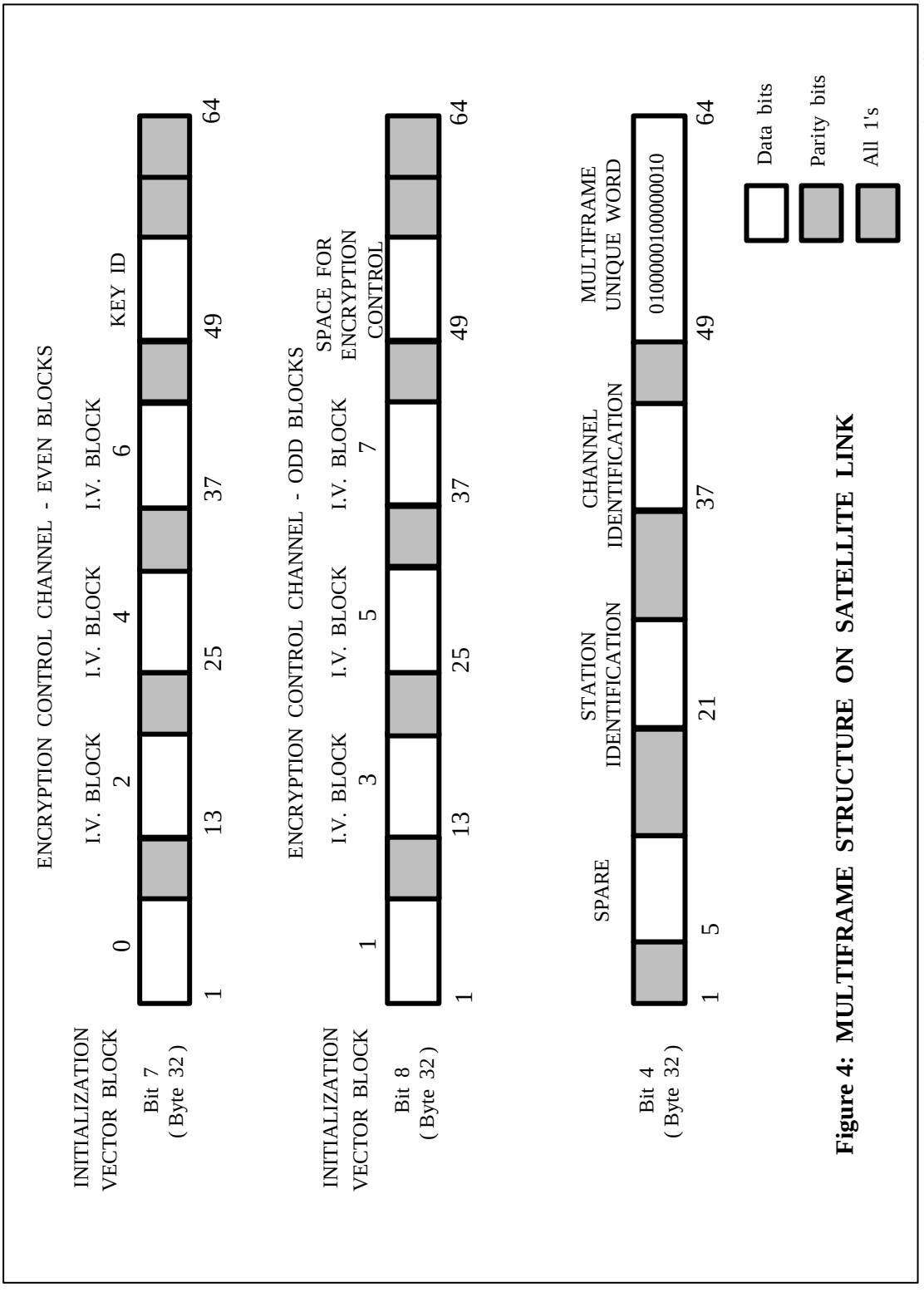
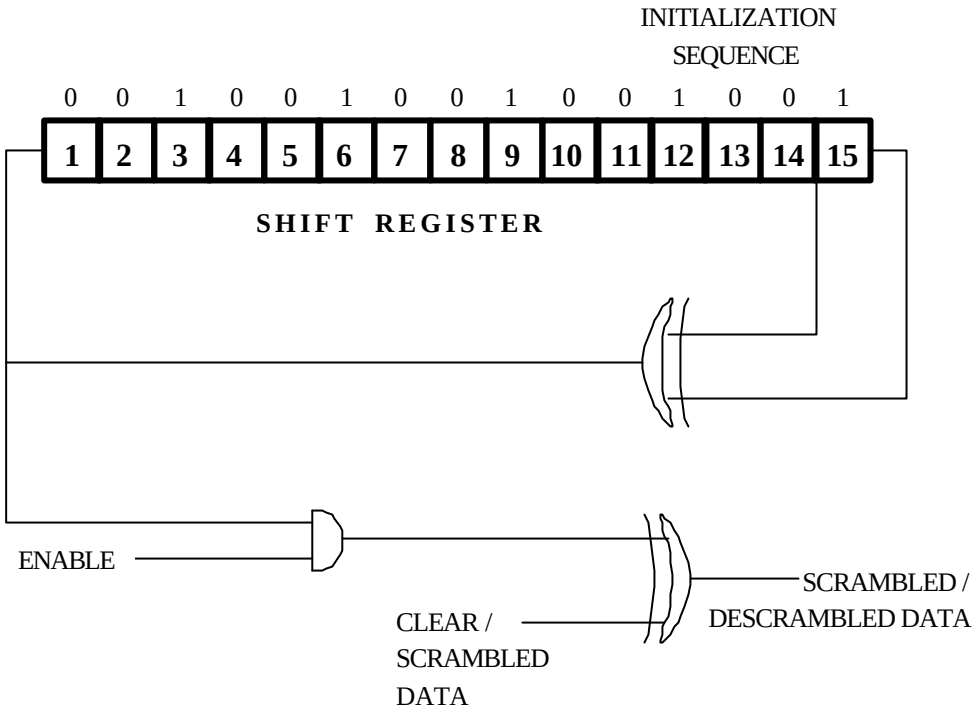


Figure 4: MULTIFRAME STRUCTURE ON SATELLITE LINK



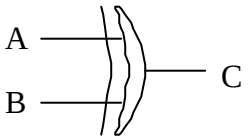
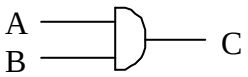
SYMBOL	FUNCTION	LOGIC TABLE A	B	C
	EXCLUSIVE OR	0	0	0
		0	1	1
		1	0	1
		1	1	0
	AND	0	0	0
		0	1	0
		1	0	0
		1	1	1

Figure 5: SYNCHRONOUS SCRAMBLER AND DESCRAMBLER SCHEMATIC

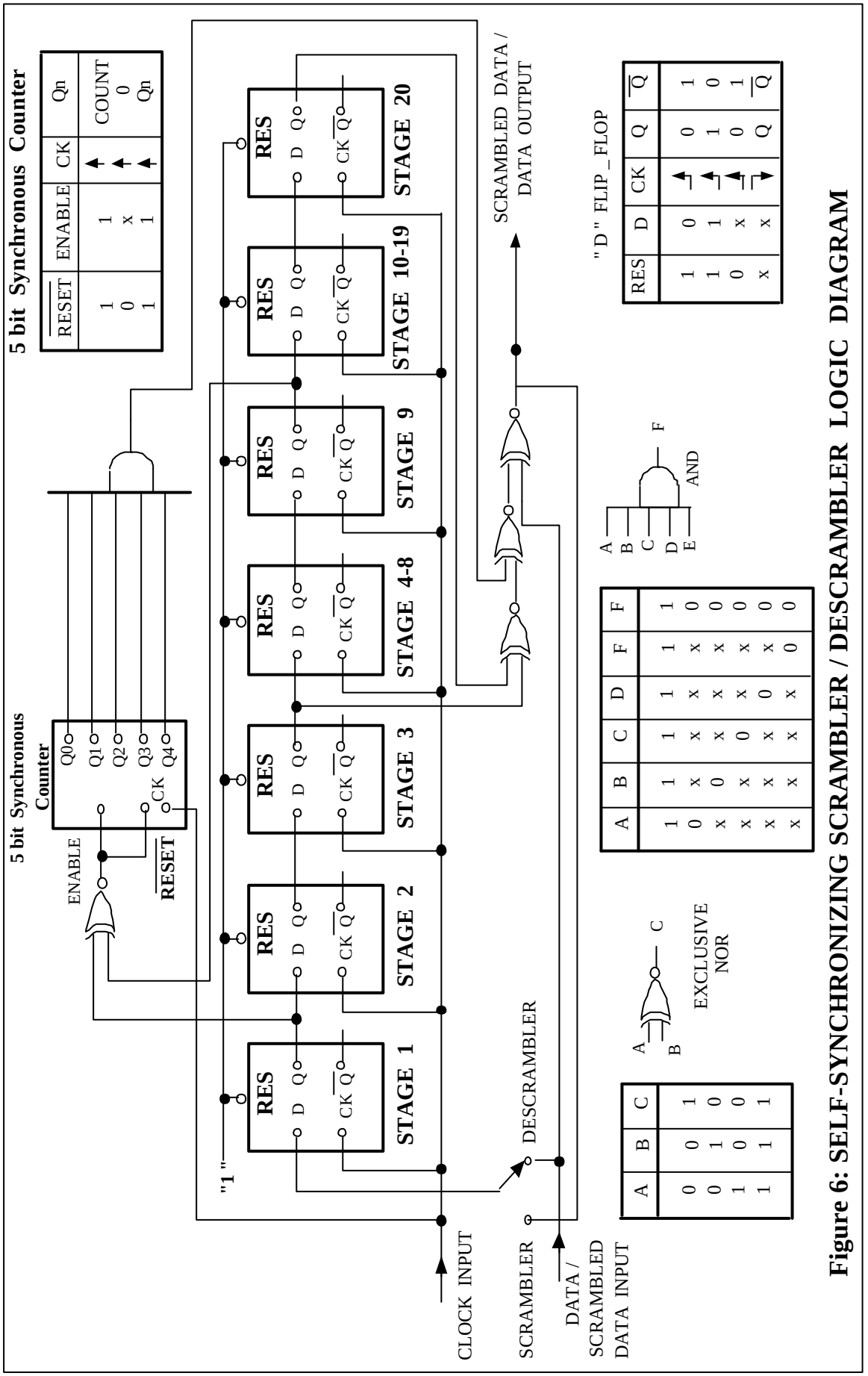
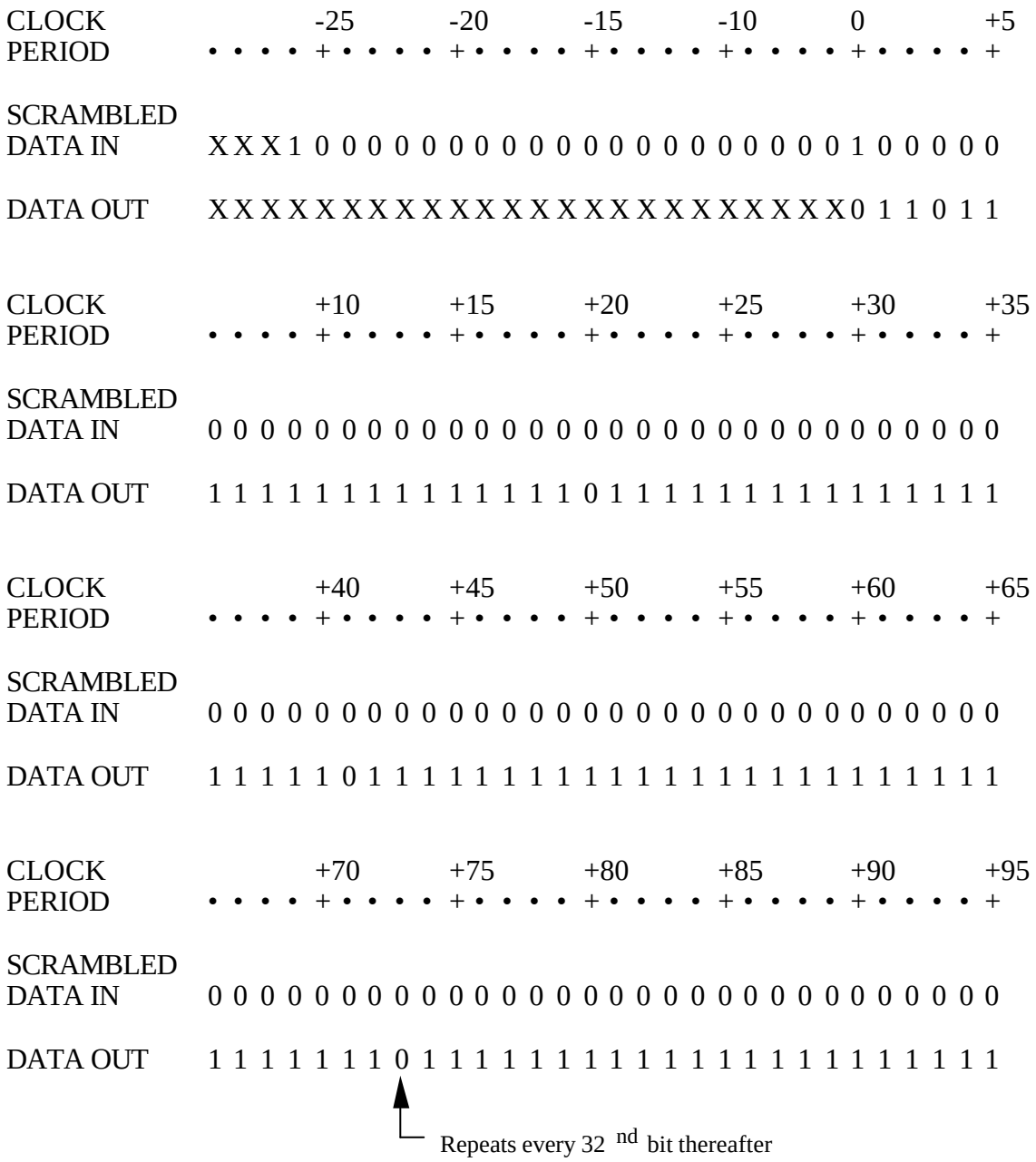


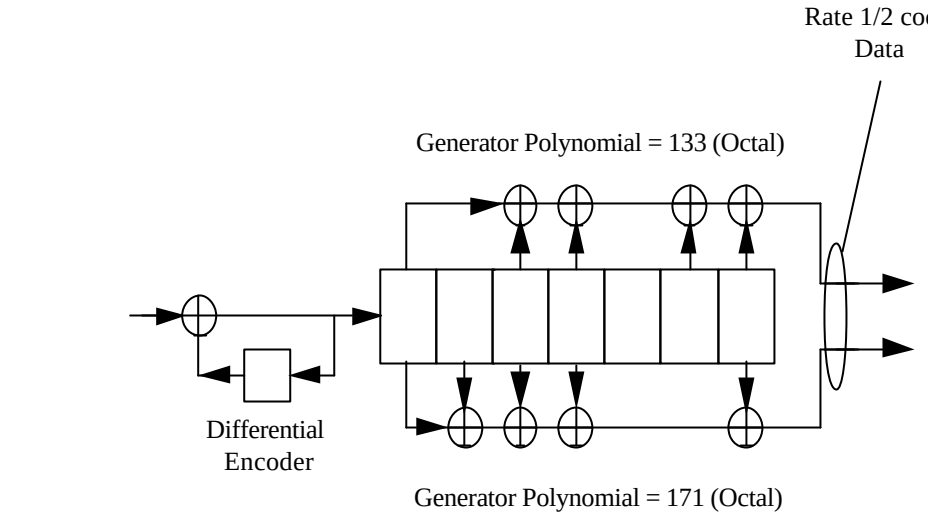
Figure 6: SELF-SYNCHRONIZING SCRAMBLER / DESCRAMBLER LOGIC DIAGRAM



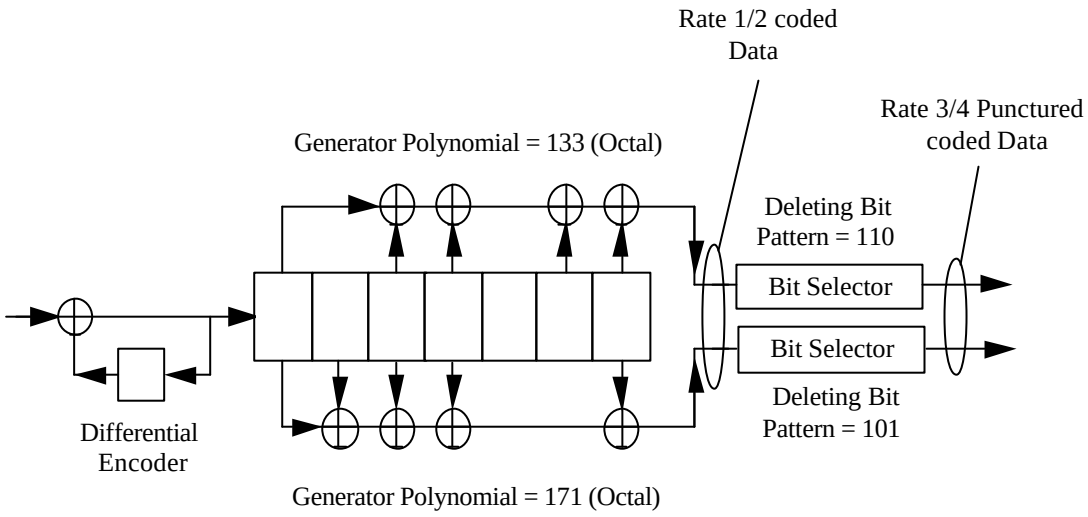
Notes:

1. x = Either 1 or 0 (don't care)
2. The purpose of the digital "one" followed by 25 "zeros" beginning at clock period -26 is to reset the 5-bit counter and "flush-out" the 20-stage shift register.

Figure 7: DIGITAL IMPULSE RESPONSE OF THE SELF-SYNCHRONIZING DESCRAMBLER



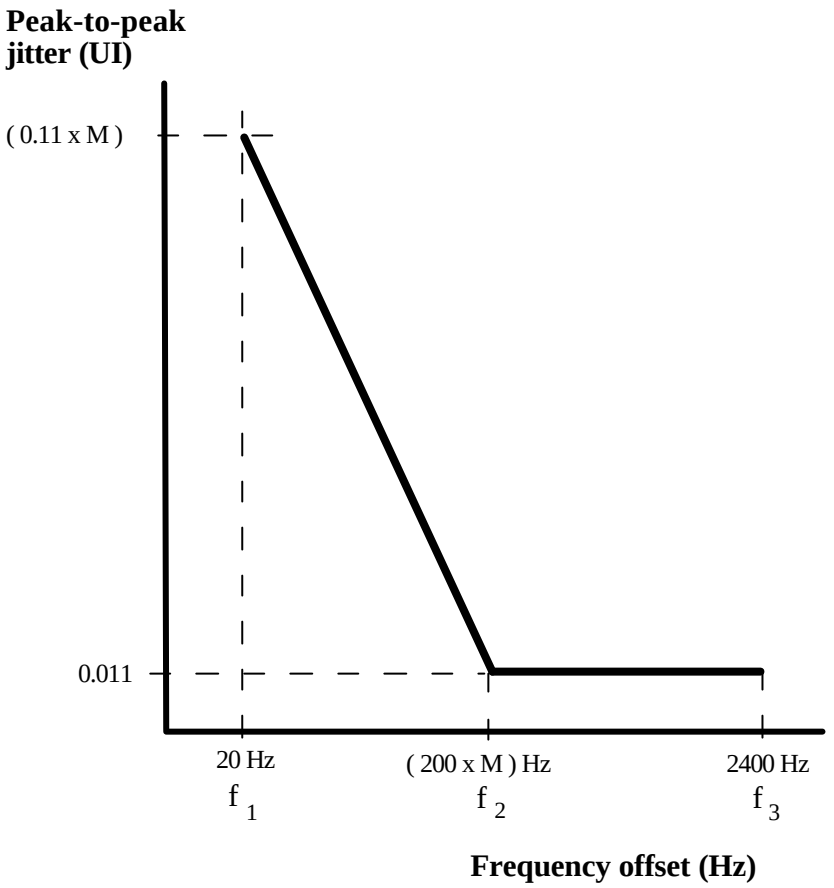
(a) Rate 1/2 FEC



(b) Rate 3/4 FEC

Notes: 1. The Symbol ⊕ denotes a modulo-2 adder
2. In the deleting bit pattern, 1 denotes transmitting and 0 denotes deleting
3. The far right-most shift register stage corresponds to the least significant bit in the Generator Polynomial

Figure 8: CONVOLUTION ENCODING PROCESS BLOCK DIAGRAM FOR USE WITH VITERBI DECODING



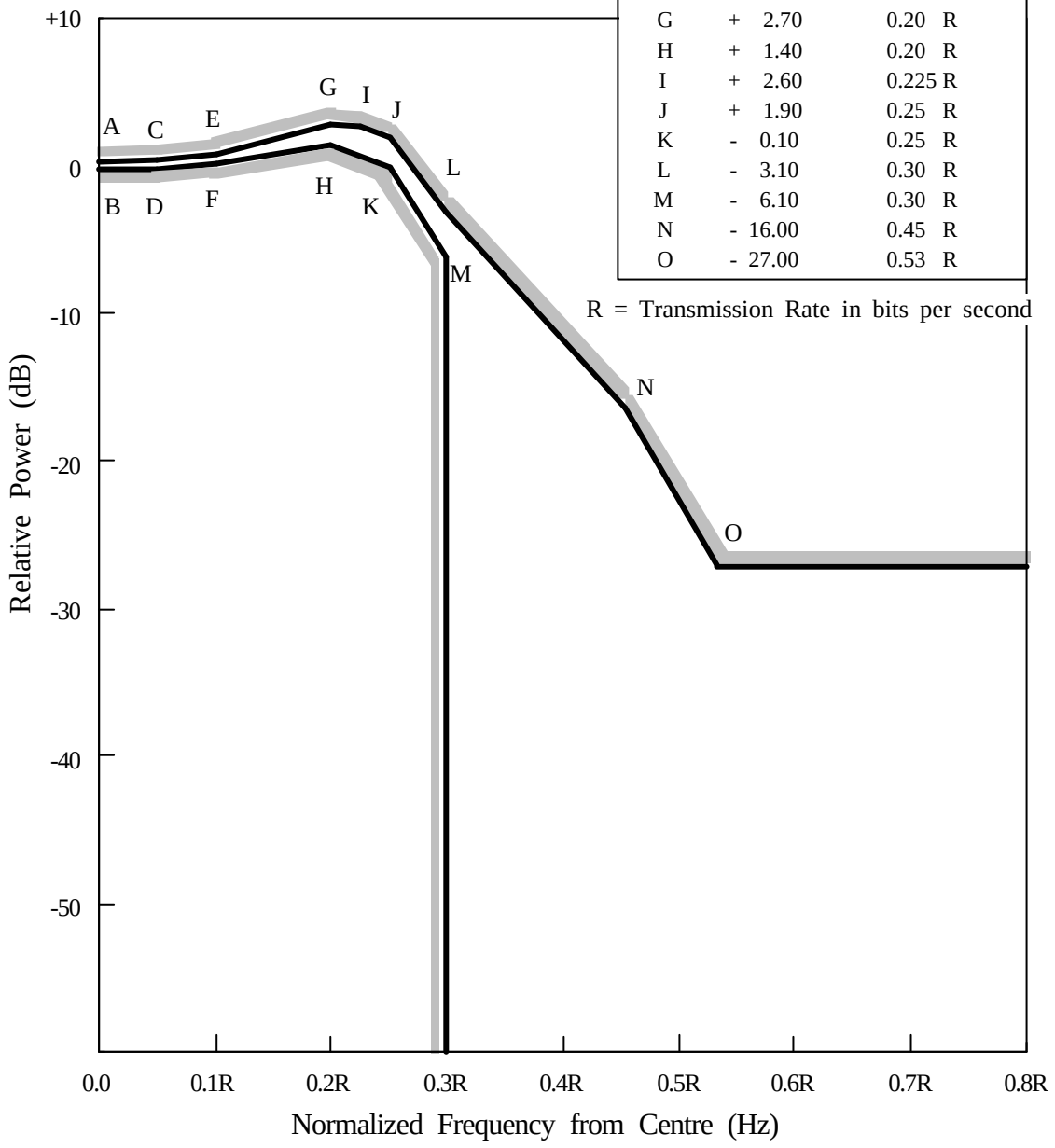
Where M = 1 for 64 kbit/s and 128 kbit/s
M = 2 for 256 kbit/s
M = 8 for 1920 kbit/s
1 UI = 360°

Figure 9: TRANSMIT SIDE CLOCK JITTER

COORDINATES OF POINTS

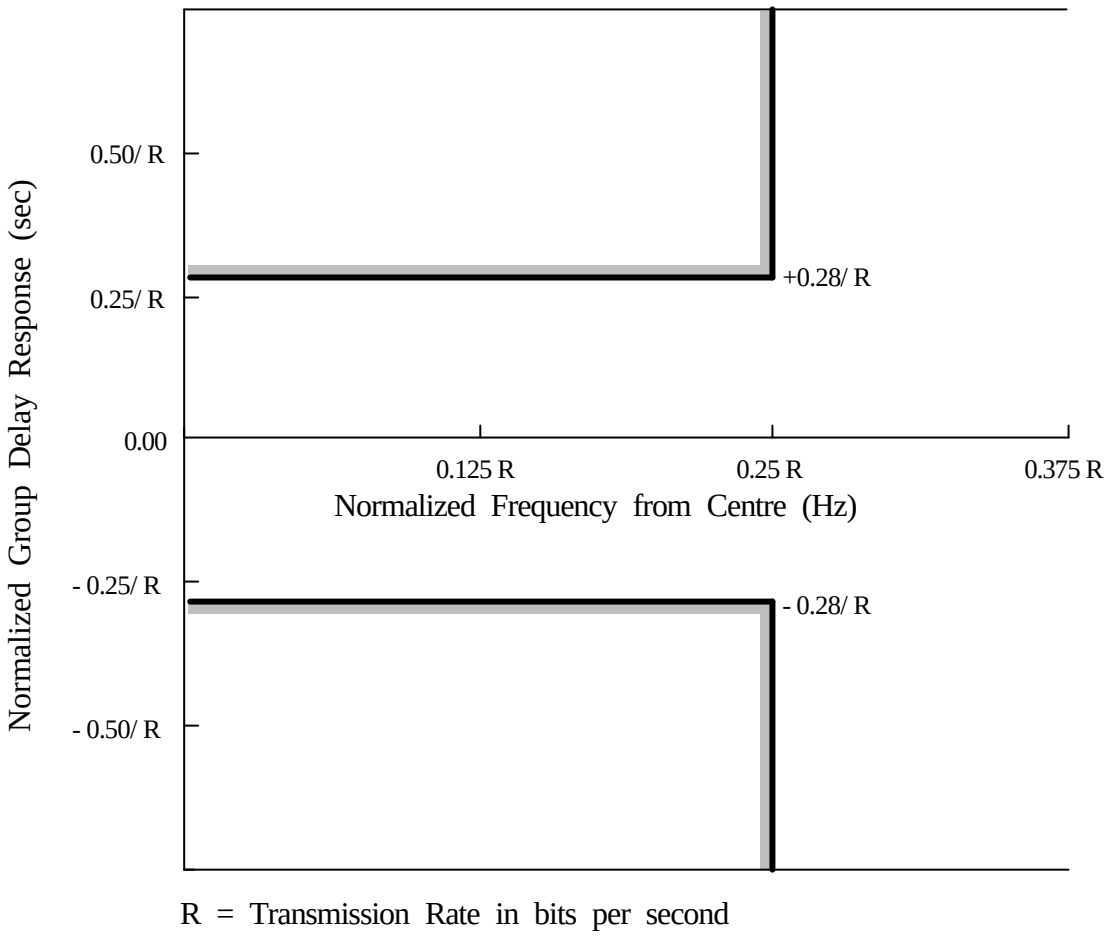
POINT	AMP. (dB)	NORM. FREQ. (Hz)
A	+ 0.25	0.0
B	- 0.25	0.0
C	+ 0.40	0.05 R
D	- 0.25	0.05 R
E	+ 0.80	0.10 R
F	+ 0.15	0.10 R
G	+ 2.70	0.20 R
H	+ 1.40	0.20 R
I	+ 2.60	0.225 R
J	+ 1.90	0.25 R
K	- 0.10	0.25 R
L	- 3.10	0.30 R
M	- 6.10	0.30 R
N	- 16.00	0.45 R
O	- 27.00	0.53 R

R = Transmission Rate in bits per second



NOTE: The filter response is not a mandatory requirement. It is used to specify the transmit spectrum, which is a mandatory requirement.

Figure 10: MODULATOR FILTER AMPLITUDE RESPONSE



NOTES :

1. The filter response is not a mandatory requirement. It is used to specify the transmitted carrier spectrum, which is a mandatory requirement.

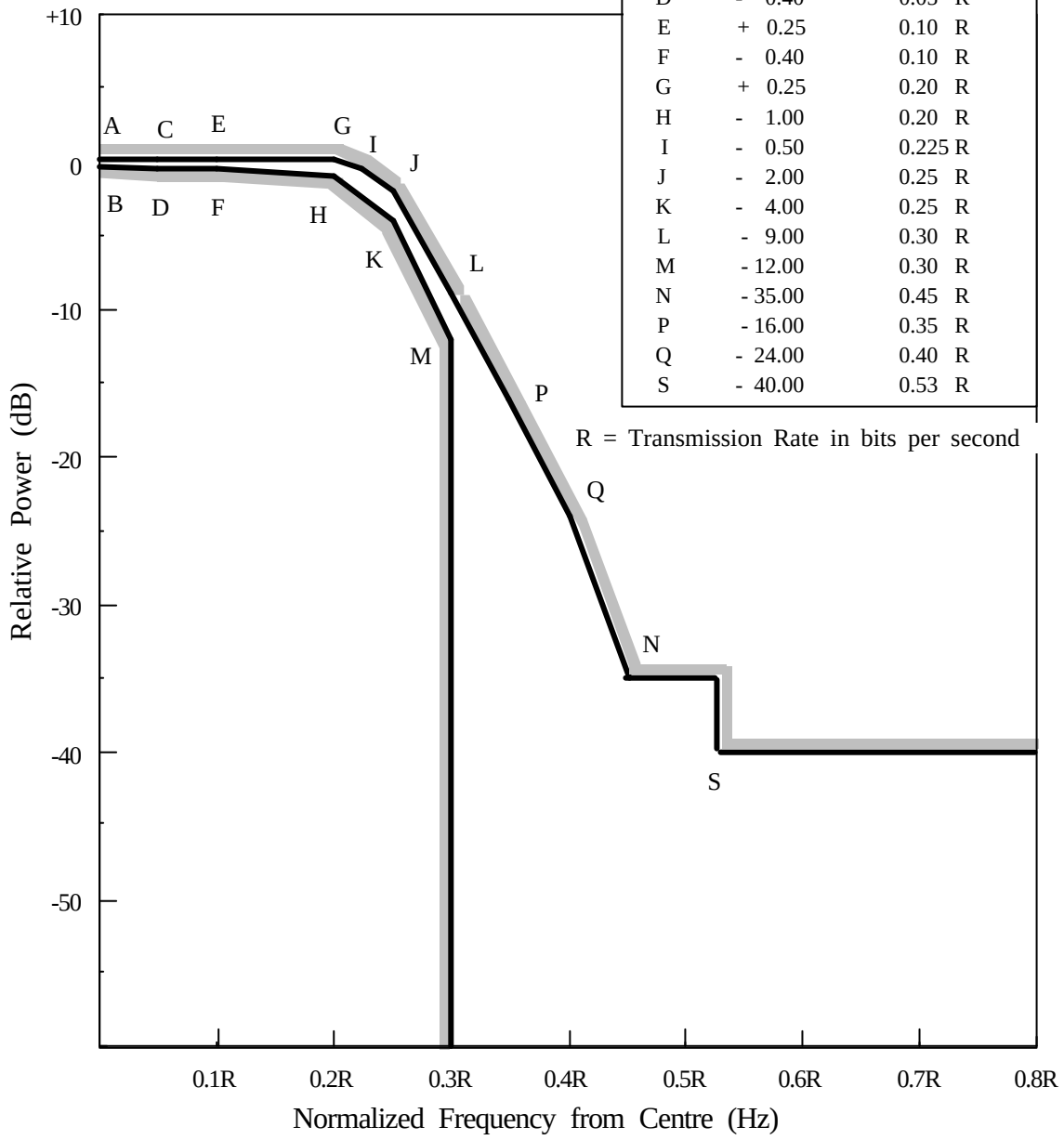
2. Either the above group delay response or a phase response with less than ± 4 degrees departure from a linear phase shift (over the frequency range ± 0.25 R Hz about the centre frequency) may be used.

Figure 11: MODULATOR AND DEMODULATOR FILTER GROUP DELAY RESPONSE

COORDINATES OF POINTS

POINT	AMP. (dB)	NORM. FREQ. (Hz)
A	+ 0.25	0.0
B	- 0.25	0.0
C	+ 0.25	0.05 R
D	- 0.40	0.05 R
E	+ 0.25	0.10 R
F	- 0.40	0.10 R
G	+ 0.25	0.20 R
H	- 1.00	0.20 R
I	- 0.50	0.225 R
J	- 2.00	0.25 R
K	- 4.00	0.25 R
L	- 9.00	0.30 R
M	- 12.00	0.30 R
N	- 35.00	0.45 R
P	- 16.00	0.35 R
Q	- 24.00	0.40 R
S	- 40.00	0.53 R

R = Transmission Rate in bits per second



NOTES:

1. Points A through N correspond to points A through N in Figure 9 Modular Filter Amplitude Response

2. 0 dB relative power corresponds to - 10 log (R/2) dB/Hz relative to the unmodulated carrier power

Figure 12: POWER SPECTRAL DENSITY MASK AT MODULATOR OUTPUT

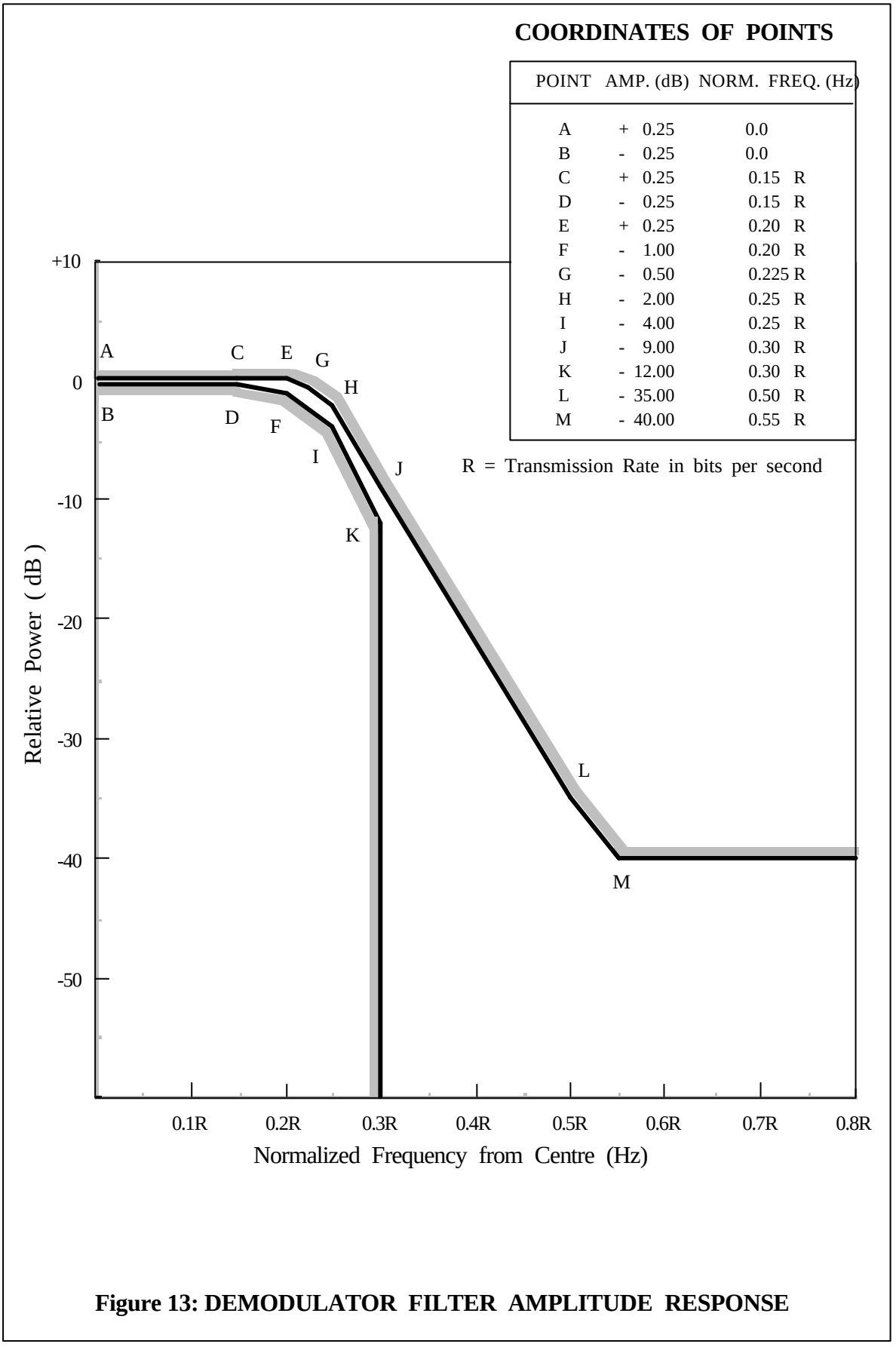


Figure 13: DEMODULATOR FILTER AMPLITUDE RESPONSE

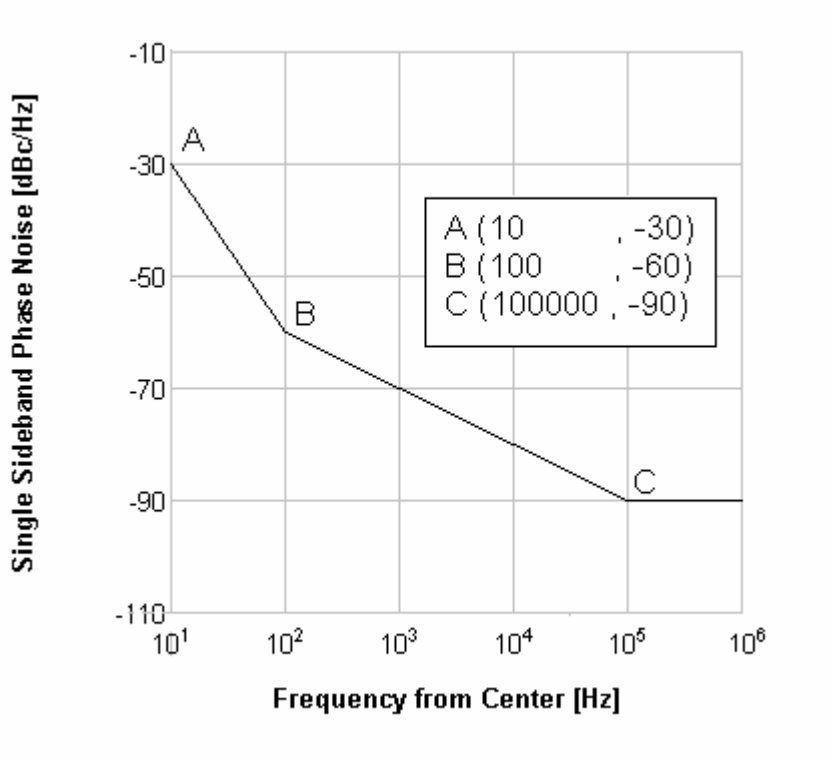


Figure 14. CONTINUOUS PHASE NOISE ON TRANSMITTED CARRIER

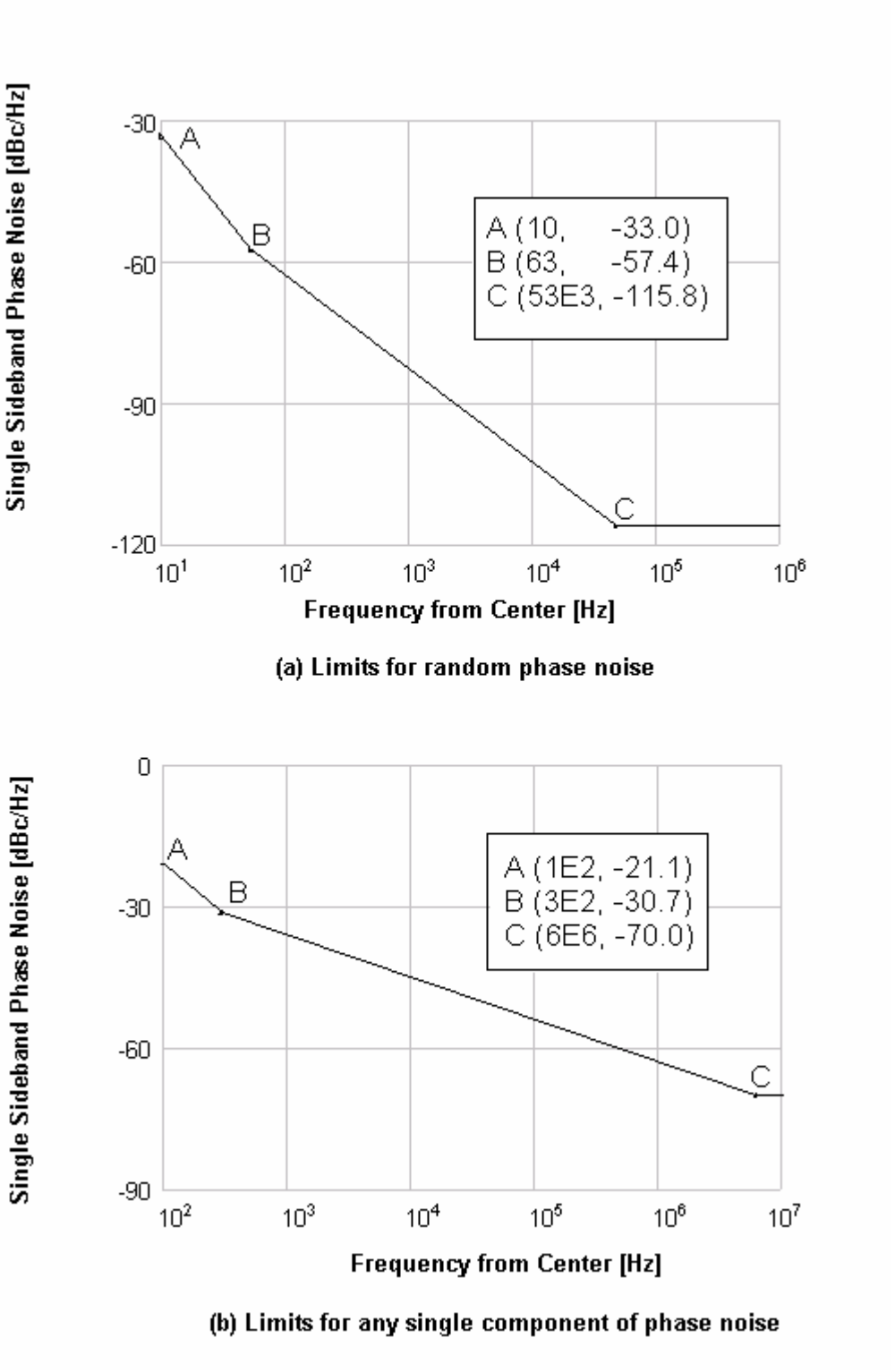


Figure 15 SATELLITE SPURIOUS MODULATION LIMITS