AMD Functional Data Sheet, 939-Pin Package

Publication #	**31411**	Revision:	**3.03**
Issue Date:	**May 2005**		

Advanced Micro Devices

Contents

List of Figures

List of Tables

Revision History

Date	Revision	Description
May 2005	3.03	Updated VDD_PON specs in Table 30. Updated TMS pin timing description in Section 7.5. Updated HyperTransport™ electrical information in Tables 13, 14, and 15. Added package drawing Figure 16. Added $T_{CONTROL}$ and T_{CASE} description in Section 7.7. Added Rev E specific information in Chapters 1 and 2. Updated HyperTransport™ electrical information in Section 7.2. Removed DRAM interface frequency table from Section 2.5.2.2 and supplemented with a reference to the document where it was moved. Updated output slew rates for DDR signals in Table 20. Revised Section 7.8.3.3 power failure requirements. Added mechanical loading information in Section 8.1.
June 2004	3.01	New document per new data sheet structuring. Specification modifications from previous document structure include: Added slew rates for some miscellaneous signals in Table 21. Clarified THERMTRIP_L operation in section 3.7. Removed CLKIN typ jitter parameter in Table 25. Removed VID encoding table. Clarified S1 hardware description and removed C3 support in Table 3. Changed thermal diode sensor requirements to two sourcing currents only in section 7.7. Added Table 26 to section 7.5 to enumerate metal mask VID[4:0] encodings for different processor revisions. Clarified DDR400 VDDIO specification in Table 30. Removed C2 from Table 3.

1 Overview

The processor is designed to support performance desktop and workstation applications. It provides single or dual core capability, a high-performance HyperTransport™ link to I/O, as well as a single 128-bit high-performance DDR SDRAM memory controller. A block diagram of the processor is shown in Figure 1.

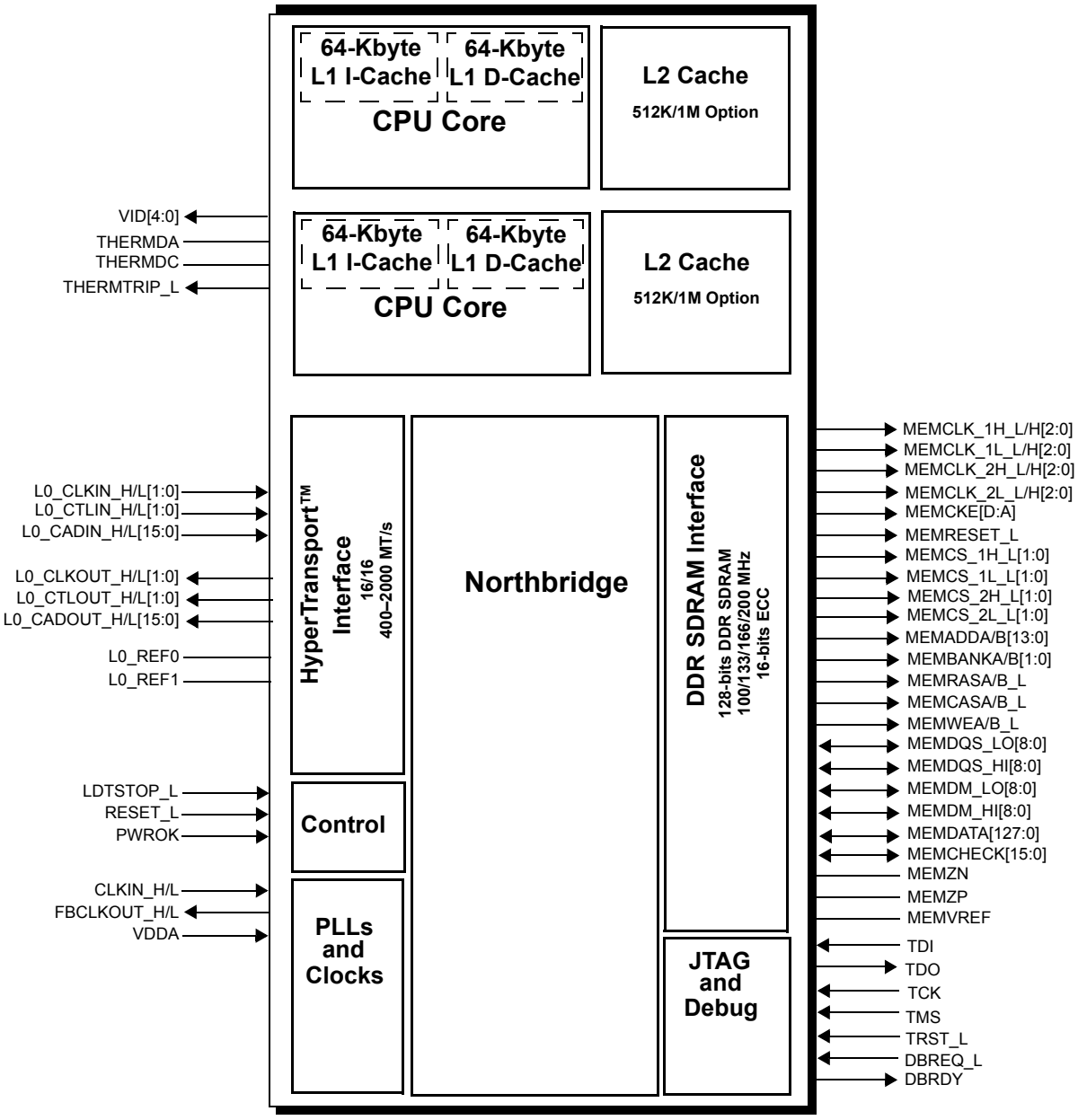


Figure 1. Processor Block Diagram

2 Functional Description

2.1 Instruction Set Support

The processor supports the standard x86-instruction set defined in the *AMD64 Architecture Programmer's Manual,* volumes 3–5, order# 24594. The processor also supports the following extensions to the standard x86 instruction set, which are described in the same volume set:

- AMD64 instructions
- MMX® and 3DNow!™ technology instructions
- SSE, SSE2, and SSE3 instructions

2.2 Multiple Core Support

The processor supports both single core and dual core options. Dual core processors have unique instances of L1 D-Cache, L1 I-Cache, and L2 Cache for each core (cache implementation is described in Section 2.3).

2.3 Internal Cache Structures

The processor implements internal caching structures as described in the following sections.

2.3.1 Level 1 Caches

The L1 data cache (L1 D-Cache) contains 64 Kbytes of storage organized as 2-way set associative. The L1 data cache is protected with ECC. Two simultaneous 64-bit operations (load, store or combination) are supported. The L1 instruction cache (L1 I-Cache) contains 64 Kbytes of storage organized as 2-way associative. The L1 Instruction Cache is protected with parity.

2.3.2 Level 2 Cache

The L2 cache contains both instruction and data stream information. It is organized as 16-way set-associative. The L2 cache data and tag store is protected with ECC. When a given cache line in the L2 cache contains instruction stream information, the ECC bits associated with the given line are used to store predecode and branch prediction information.

2.4 Error Handling (Machine Check)

The processor implements the standard x86 machine check architecture as defined in the *AMD64 Architecture Programmer's Manual,* Volume 2, order# 24593, and the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094.

The machine check architecture is defined with ECC single-bit detection/correction and double-bit detection for the following arrays:

- L1 Data Cache Storage
- L2 Data Cache Storage
- L2 Data Cache Tag
- Instruction Cache
- DRAM (see "Memory Controller" on page 15).

2.5 Northbridge

The Northbridge logic in the processor refers to the HyperTransport™ technology interface, the memory controller, and their respective interfaces to the CPU core. These interfaces are described in more detail in the following sections.

2.5.1 HyperTransport™ Technology Overview

The processor includes a 16-bit HyperTransport™ technology interface designed to be capable of operating up to 2000 mega-transfers per second (MT/s), resulting in a bandwidth of up to 8 Gbytes/s (4 Gbytes/s in each direction). The processor supports HyperTransport™ synchronous clocking mode. Refer to the *HyperTransport™ I/O Link Specification* (www.hypertransport.org) for details of link operation.

2.5.1.1 Link Initialization

The HyperTransport™ technology interface of the processor can be operated as a single 16-bit link. The *HyperTransport™ I/O Link Specification* details the negotiation that occurs at power-on to determine the widths and rates that will be used with the link. Refer also to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094, for information about link initialization and setup of routing tables.

The unused L0_CTLIN_H/L[1] pins must be terminated as follows:

- L0_CTLIN_H[1] must be pulled High.
- L0_CTLIN_L[1] must be pulled Low.

Refer to the *AMD Athlon™ 64 939 Motherboard Design Guide,* order# 30474*,* for details on the proper HyperTransport™ technology signal termination resistor values.

2.5.1.2 HyperTransport™ Technology Transfer Speeds

The HyperTransport™ link of the processor is capable of operating at 200, 400, 600, 800, and 1000 MHz (400, 800, 1200, 1600, and 2000 MT/s respectively). The link transfer rate is determined during the software configuration of the system, as specified in the *HyperTransport™ I/O Link Specification*. The maximum transfer rate and bandwidth for the processor's HyperTransport™ technology interface is 2000 MT/s, with a maximum bandwidth of 8 Gbytes/s (4 Gbytes/s in each direction).

2.5.2 Memory Controller

The processor's memory controller provides a programmable interface to a variety of standard DDR SDRAM DIMM configurations. The following features are supported:

- Self-Refresh mode
- Up to four unbuffered DIMMs in a 128-bit configuration, or up to two unbuffered DIMMs in a 64-bit configuration
- The controller provides programmable control of DRAM timing parameters to support the following memory speeds:
  - — 100-MHz (DDR200) PC-1600 DIMMs
  - — 133-MHz (DDR266) PC-2100 DIMMs
  - — 166-MHz (DDR333) PC-2700 DIMMs
  - — 200-MHz (DDR400) PC-3200 DIMMs
- 2T timing option to accommodate loading of unbuffered DIMMs
- DRAM devices that are 8 and 16 bits wide.
- DIMM sizes from 32 Mbytes (using 64Mb x16 DRAMs) to 1 Gbyte.
- Interleaving memory within DIMMs.
- ECC checking with double-bit detect with single-bit correct.
- May be configured for 32-byte or 64-byte burst length (32-byte mode applies only when operating with a 64-bit DRAM interface).
- Programmable page-policy:
  - — Support of up to sixteen open pages total across all chip-selects
  - — Statically idle open-page time
  - — Optional dynamic precharge control based on page-hit/miss history

For programming information and specific details of these features, refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094.

2.5.2.1 Memory Pin Interface

Some processor pin names have 'A' and 'B' suffixes. This is a way to distinguish between two otherwise functionally identical pins that exist as multiple redundant pins to accommodate loading. This is normally the case for address and control pins in unbuffered systems. MEMBANKB[1:0] and MEMADDB[13:0] are different in that they are not logically redundant with their 'A' signal counterparts. During precharges, activates, reads and writes, MEMBANKB[1:0] is logically inverted from MEMBANKA[1:0], and MEMADDB[13:0] is inverted from MEMADDA[13:0] except for bit 10 (which is the auto-precharge bit). In other words, whenever these pins are acting as addresses, they are inverted to minimize switching noise on the motherboard. An example of when they are not inverted would be during initialization when these wires carry data for the Mode Register Set commands.

The controller supports 64-bit operation (72-bits including ECC) or 128-bit ganged operation (144-bits including ECC). When configured for 128-bits, the upper and lower chip-selects are logically equivalent signals to provide adequate buffering to drive four DIMMs. DIMMs must be populated in matched pairs when configured for 128-bit mode. Figure 2 illustrates the typical DIMM connections in a 128-bit system with ECC support.

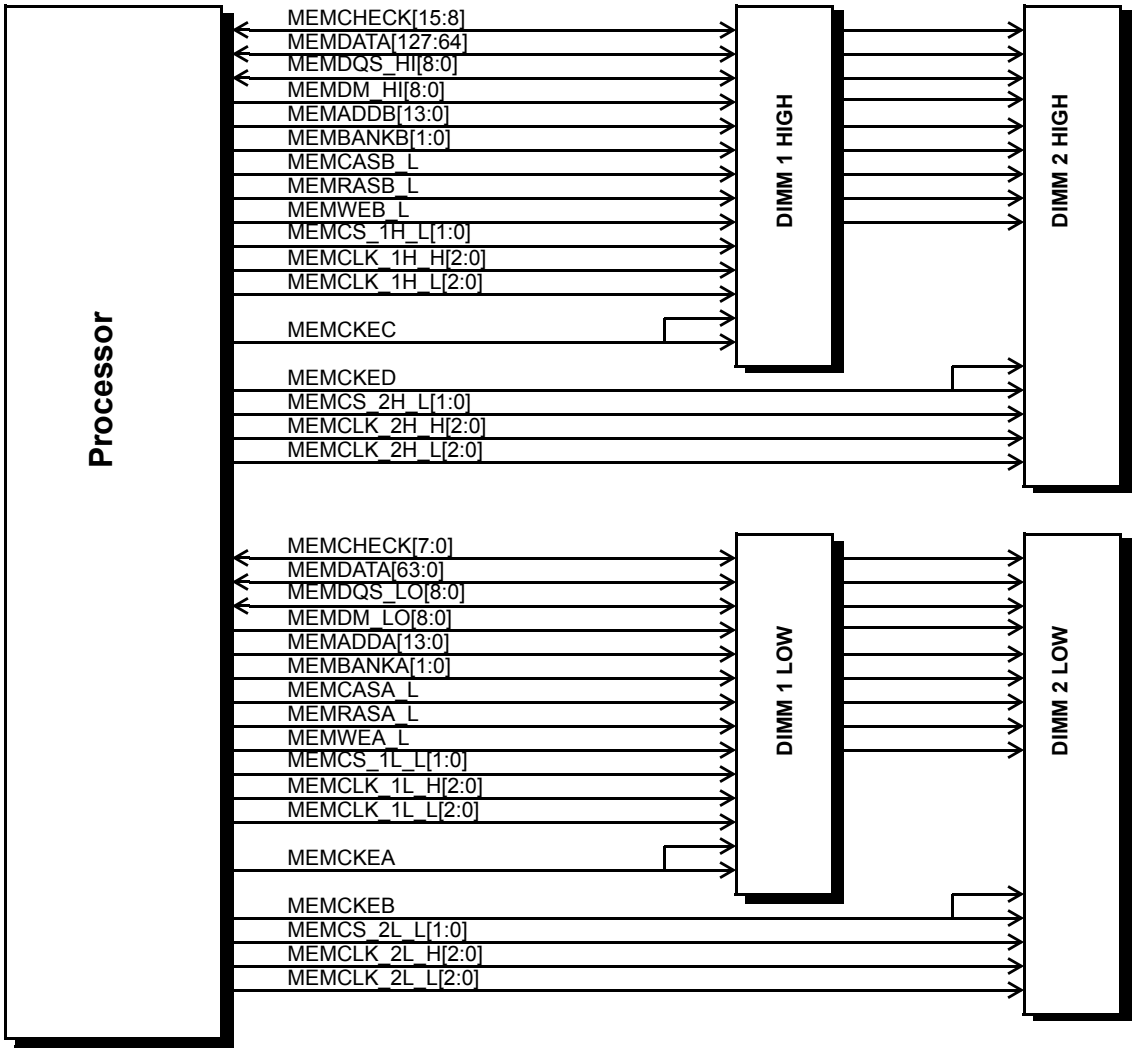


Figure 2. DIMM Connections in 128-bit Mode

2.5.2.2 DRAM Operation

At power-on reset, the MEMCKE* pins are driven low while the processor PLLs are ramping. Clocks are driven on the MEMCLK* pins only after BIOS programs the appropriate clock ratio value in the memory controller configuration registers. The actual DRAM frequency may vary based on the CPU clock multiplier and other configuration options (the memory controller automatically adjusts refresh counters at all speeds as required to meet the device refresh specifications). Refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094, for details on actual DRAM frequencies for specific configurations and processor frequencies.

The use of 2T timing allows support of many DIMM combinations at maximum DDR speeds. The 2T timing feature causes commands and addresses to be driven for two clock cycles and qualified with

an associated chip select on the second clock cycle, allowing an extra clock of setup to accommodate heavy DIMM loading (such as double-rank DIMMs). Refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094, for the DIMM combinations that require 2T timing to operate at the full DRAM speed.

Refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094, for supported DRAM speeds under specific loading conditions.

Table 1 on page 18 lists the maximum memory sizes per chip-select for the various supported DRAM device configurations. Note that for DIMMs using two chip-selects, the total memory size per DIMM is doubled. Refer to the *AMD Athlon™ 64 939 Motherboard Design Guide,* order# 30474*,* for details on the connection scheme for unbuffered DIMMs.

Table 1. Total Memory Sizes Per Chip Select

Devices Used on DIMMs	Size Per CS
64 M-bit (2M x8-bits x4 banks)	64 Mbyte
64 M-bit (1M x16-bits x4 banks)	32 Mbyte
128 M-bit (4M x8-bits x4 banks)	128 Mbyte
128 M-bit (2M x16-bits x4 banks)	64 Mbyte
256 M-bit (8M x8-bits x4 banks)	256 Mbyte
256 M-bit (4M x16-bits x4 banks)	128 Mbyte
512 M-bit (16M x8-bits x4 banks)	512 Mbyte
512 M-bit (8M x16-bits x4 banks)	256 Mbyte
1 G-bit (32M x8-bits x4 banks)	1 Gbyte
1 G-bit (16M x16-bits x4 banks)	512 Mbyte

The controller supports programmable timing and refresh as described in the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094. Auto-refresh is supported and is staggered by t_{RFC} across chip-selects to reduce system noise. Unpopulated DIMM slots are not refreshed.

2.5.2.3 DRAM Power Management

The memory controller supports self-refresh mode to accommodate various power management states such as ACPI C3, S1, and S3 states.

2.5.2.4 Main Memory Hardware Scrubbing

The memory controller scrubs the main memory arrays to prevent the build up of soft errors. Any correctable or non-correctable errors are logged to the machine check logs and can be programmed to

invoke the machine check interrupt. The scrubbing function can be used in three modes as described in the following sections.

2.5.2.4.1 Sequential Scrubbing

In this mode, the scrubber sequentially proceeds through main memory, performing a read-write cycle or a read-modify-write cycle if a correctable error is found. The scrubber scrubs one cache line on each scrub interval that is programmable from 40 ns to 84 ms.

2.5.2.4.2 Source Correction Scrubbing

In this mode, the scrubber is directed to scrub any cache line that is the source of any corrected error during normal accesses. During normal operation when source correction scrubbing is disabled, single-bit errors are corrected on the fly and the corrected data is passed without updating the source memory location. When source scrubbing is enabled the scrubber also corrects the source memory location.

2.5.2.4.3 Sequential Plus Source Correction Scrubbing

When both sequential and source correction scrubbing are enabled, the scrubber sequentially proceeds through main memory. If a correctable error is detected during normal operation, the scrubber is redirected to the location of the error, and after it corrects that location in main memory it resumes sequential scrubbing at the previous location

3 Power Management

The processor provides the following power management features designed to be compliant with the Advanced Configuration and Power Interface (ACPI) Specification and HyperTransport™ technology:

- Halt state with associated programmable power savings
- STPCLK/Stop Grant protocol capable of supporting eight distinct versions of Stop Grant
- LDTSTOP_L signal support
- Memory controller and host bridge power management
- Processor Performance state (P-State) transition support
- Voltage plane isolation based upon PWROK signal
- Low-power state while RESET_L signal is asserted
- On-die thermal diode

Table 2 maps processor capabilities to ACPI states.

Table 2. Processor Capabilities Mapped to ACPI States

ACPI State	Processor
Processor P-States	Processor P-state transitions are supported on some versions of the processor.
C1	Halt
Passive Cooling	Passive Cooling is supported by Stop Grant (throttling) and/or P-state transitions.
C3	Not supported.
S1	Stop Grant. In response to LDTSTOP_L assertion the processor's HyperTransport™ link is disconnected, memory is placed in self-refresh mode, and the host bridge and memory controller are placed into a low-power state.
S3	Processor core and HyperTransport™ technology voltage planes are not powered. DDR SDRAM interface remains powered and holds memory in self-refresh mode.
S4, S5, G3	All power is removed from the processor.

3.1 Halt

When the HLT instruction is executed, the processor stops program execution and issues a Halt special cycle. The power savings associated with the Halt state are determined by configuration registers in the processor (refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094, for details of these configuration registers). The CPU clock grid frequency can be divided down in the absence of probe activity that would force the processor's caches to be snooped.

The CPU clock grid is automatically brought to full frequency when probe activity is present and returned to the low-power state when probe activity ceases.

If a STPCLK assertion message is received while the processor is in the Halt State, the processor enters the Stop Grant state and issues a Stop Grant special cycle. When a STPCLK deassertion message is received, the processor exits the Stop Grant state and returns to the Halt State.

The processor exits the Halt State in response to PWROK deassertion, RESET_L assertion, INIT, NMI, SMI, or any unmasked interrupt received over the HyperTransport™ link.

3.2 STPCLK/Stop Grant

When the processor recognizes the STPCLK assertion message, it enters the Stop Grant state on the next instruction boundary and issues a Stop Grant special cycle. The power savings associated with the Stop Grant state is determined by configuration registers in the processor. The power savings mechanisms associated with the Stop Grant state include the following:

- CPU clock grid divisor applied in the absence of probe activity. If probe activity that requires a cache snoop occurs while the processor is in the Stop Grant state, the clock grid is ramped back up to service the probe. When probe activity ceases, the CPU clock grid is ramped back down again.
- Placing system memory into self-refresh mode in response to LDTSTOP_L signal assertion.
- Ramping the processor host bridge/memory controller clock grid down in response to LDTSTOP_L signal assertion.
- Processor performance state transition in response to LDTSTOP_L signal assertion.
- Changing HyperTransport™ link width and/or link frequency in response to LDTSTOP_L signal assertion.

The processor exits the Stop Grant state when it receives the following:

- A STPCLK deassertion message.
- RESET_L pin asserted, or an INIT assertion message.

- PWROK is deasserted.

If the LDTSTOP_L signal is asserted after the processor is in the Stop Grant state, then LDTSTOP_L must be deasserted, and the HyperTransport™ link must be re-initialized before a STPCLK deassertion message can be received by the processor to bring the processor out of the Stop Grant state.

The processor's host bridge ensures that STPCLK messages are passed to the CPU prior to the subsequent I/O response to the cycle that caused STPCLK assertion, as long as the subsequent I/O response message has the PassPW bit clear and the Unit ID of the response matches the Unit ID of the STPCLK message.

3.3 Processor Performance State Transitions

Some versions of the processor support processor performance state (P-State) transitions. Processor P-States are valid combinations of processor voltage and frequency. P-State transitions are performed through the FID_Change protocol. The processor provides two Model-Specific Registers (MSRs) in support of the FID_Change protocol: the FIDVID_CTL and FIDVID_STATUS MSRs. The FIDVID_CTL MSR allows software to dictate what P-State the processor will transition to, and to initiate the transition to that state. The FIDVID_STATUS MSR allows software to determine when a P-State transition is complete.

P-state transitions are comprised of multiple FID-only and VID-only transitions as described in *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094. Refer to the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet,* order# 30430*,* for a list of the valid P-States for this processor.

During VID only transitions, no HyperTransport™ FIDVID_Change system management message is issued when the processor's FIDVID_CTL MSR's FidVidChangeInitiate bit is set. The processor is not put into Stop Grant, but rather drives the new VID while the processor continues to execute instructions.

The following describes a FID-only transition:

- When the processor's FIDVID_CTL MSR's FidVidChangeInitiate bit is set, the processor issues a FID_Change special cycle.

- When the processor subsequently receives a STPCLK message, it enters the Stop Grant state and issues a Stop Grant special cycle with a System Management Action Field (SMAF, bits 3:1 of the system management command field) corresponding to the SMAF received with the STPCLK message.

Note: *If two STPCLK messages are issued before the processor issues a Stop Grant special cycle, the SMAF issued will correspond to the last STPCLK message received.*

- When the processor's host bridge broadcasts the Stop Grant special cycle with a SMAF indicating FID/VID change down its HyperTransport™ link(s), the processor is primed to transition its core frequency or core voltage in response to LDTSTOP_L assertion.
- When the LDTSTOP_L pin is asserted, the processor performs the following steps:
  - — Disconnects its HyperTransport™ link(s)
  - — Places system memory into self-refresh mode
  - — Ramps its entire clock grid, including host bridge and memory controller, down by a programmable value
  - — Transitions its core frequency
- When the frequency transition is complete and LDTSTOP_L is deasserted, the processor performs the following steps:
  - — Ramps its host bridge and memory controller clock grid back up to full frequency
  - — Brings system memory out of self-refresh mode
  - — Reconnects its HyperTransport™ link(s)
- When a STPCLK deassertion message is received, the CPU clock grid is ramped up to full operating frequency, and the processor exits the Stop Grant state.

Refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094, for the detailed P-state transition algorithm. Refer to the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet,* order# 30430, to determine support for processor P-state transitions.

3.4 PWROK

When PWROK is deasserted, the processor performs the following steps:

- Isolates its VDDIO- and VTT-powered logic from all other internal logic to prevent leakage current paths between power planes.
- Tristates all DDR SDRAM I/O pins except for the MEMCKEA/B and MEMRESET_L outputs, which are driven Low.
- Drives its VID[4:0] outputs to the value that selects the startup core voltage level.

3.5 RESET_L

When RESET_L is asserted, the processor performs the following steps:

- The processor core is held in a low-power state.

- The MEMCKE[D:A] outputs are forced Low.

After RESET_L is deasserted, BIOS must program the appropriate clock divisor in the memory controller configuration registers, causing the MEMCLK_H/L[7:0] clocks to be driven. Refer to "Power-Up Signal Sequencing" on page 72 for details of RESET_L sequencing during initial power-on.

3.6 Thermal Diode

The processor provides an on-die thermal diode with anode and cathode brought out to processor pins. This diode can be read by an external temperature sensor to determine the processor's temperature. Refer to the *AMD Athlon™ 64 939 Motherboard Design Guide,* order# 30474, for details on connecting the thermal diode.

3.7 THERMTRIP_L

The processor provides a hardware-enforced thermal protection mechanism. When the processor's die temperature exceeds a specified temperature, the processor is designed to stop its internal clocks and assert the THERMTRIP_L output.

THERMTRIP_L assertion is only valid when PWROK is asserted and RESET_L is deasserted.

THERMTRIP_L assertion indicates the processor die temperature has exceeded normal operating parameters. PWROK must be deasserted in response to a THERMTRIP_L assertion to enable proper processor operation.

Once asserted THERMTRIP_L remains asserted until RESET_L is asserted.

If the processor's die temperature still exceeds the thermal trip point when RESET_L is deasserted, THERMTRIP_L will immediately be reasserted and the processor's internal clocks stop.

4 Connection Diagrams

The pinout for the processor is illustrated in this chapter, and is divided into two parts. Figure 3 on page 28 shows the left-hand side of the top view, which is the HyperTransport™ technology interface. Figure 4 on page 29 shows the right-hand side of the top view, the DDR SDRAM interface.

The pin designations are defined in Chapter 5. Table 3 on page 32 lists the pins alphabetically by pin name.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A			VDDA	NC_A4	NC_A5	DBREQ_L	VSS	CLKIN_H	VSS	VID[0]	VID[1]	VID[3]	VID[4]	VTT_A14	MEMDATA[68]	MEMDM_UP[0]
B			VDDA	NC_B4	VDD	LDTSTOP_L	VSS	CLKIN_L	VSS	VDD	DBRDY	VDD	STRAP_LO_B13	VTT	MEMDATA[64]	VDDIO
C	L0_REF0	VSS	VDDA	NC_C4	NC_C5	NC_C6	NC_C7	VSS	VSS	STRAP_LO_C10	NC_C11	VID[2]	NC_C13	VTT	MEMDATA[69]	MEMDATA[0]
D	L0_REF1	VSS	VSS	NC_D4	VSS	VSS	VSS	NC_D8	VSS	VDD	NC_D11	NC_D12	VSS	VTT	MEMDATA[65]	VSS
E	VLDT_A	VLDT_A	VSS	VSS	COREFB_H	COREFB_L	CORESENSE	PWROK	NC_E9	VSS	STRAP_HI_E11	VSS	FBCLKOUT_L	VTT	MEMDATA[4]	MEMDATA[5]
F	VLDT_A	VLDT_A			VSS	VSS	VSS	RESET_L	VSS	VSS	STRAP_LO_F11	VSS	FBCLKOUT_H	VSS	MEMVREF	VSS
G	L0_CADIN_H[1]	L0_CADIN_L[0]	L0_CADIN_H[0]	VSS	L0_CADIN_H[8]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC_G15	MEMDATA[1]
H	L0_CADIN_L[1]	VDD	L0_CADIN_H[9]	L0_CADIN_L[9]	L0_CADIN_L[8]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
J	L0_CADIN_H[3]	L0_CADIN_L[2]	L0_CADIN_H[2]	VDD	L0_CADIN_H[10]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
K	L0_CADIN_L[3]	VSS	L0_CADIN_H[11]	L0_CADIN_L[11]	L0_CADIN_L[10]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
L	L0_CADIN_H[4]	L0_CLKIN_L[0]	L0_CLKIN_H[0]	VSS	L0_CLKIN_H[1]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
M	L0_CADIN_L[4]	VDD	L0_CADIN_H[12]	L0_CADIN_L[12]	L0_CLKIN_L[1]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
N	L0_CADIN_H[6]	L0_CADIN_L[5]	L0_CADIN_H[5]	VDD	L0_CADIN_H[13]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
P	L0_CADIN_L[6]	VSS	L0_CADIN_H[14]	L0_CADIN_L[14]	L0_CADIN_L[13]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
R	L0_CTLIN_H[0]	L0_CADIN_L[7]	L0_CADIN_H[7]	VSS	L0_CADIN_H[15]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
T	L0_CTLIN_L[0]	VDD	STRAP_HI_T3	STRAP_LO_T4	L0_CADIN_L[15]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
U	L0_CADOUT_L[7]	L0_CTLOUT_H[0]	L0_CTLOUT_L[0]	VDD	NC_U5	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
V	L0_CADOUT_H[7]	VSS	L0_CADOUT_L[15]	L0_CADOUT_H[15]	NC_V5	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
W	L0_CADOUT_L[5]	L0_CADOUT_H[6]	L0_CADOUT_L[6]	VSS	L0_CADOUT_L[14]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
Y	L0_CADOUT_H[5]	VDD	L0_CADOUT_L[13]	L0_CADOUT_H[13]	L0_CADOUT_H[14]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AA	L0_CLKOUT_L[0]	L0_CADOUT_H[4]	L0_CADOUT_L[4]	VDD	L0_CADOUT_L[12]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AB	L0_CLKOUT_H[0]	VSS	L0_CLKOUT_L[1]	L0_CLKOUT_H[1]	L0_CADOUT_H[12]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AC	L0_CADOUT_L[2]	L0_CADOUT_H[3]	L0_CADOUT_L[3]	VSS	L0_CADOUT_L[11]	VSS			VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AD	L0_CADOUT_H[2]	VDD	L0_CADOUT_L[10]	L0_CADOUT_H[10]	L0_CADOUT_H[11]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AE	L0_CADOUT_L[0]	L0_CADOUT_H[1]	L0_CADOUT_L[1]	VDD	L0_CADOUT_L[9]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIOSENSE	VSS	MEMZP	MEMDATA[63]
AF	L0_CADOUT_H[0]	VSS	L0_CADOUT_L[8]	L0_CADOUT_H[8]	L0_CADOUT_H[9]	VSS	VSS	TRST_L	VSS	STRAP_LO_AF10	VSS	STRAP_HI_AF12	VTT_SENSE	VSS	MEMZN	VSS
AG	VLDT_B	VLDT_B	VLDT_B	VLDT_B	VSS	TMS	TCK	TDO	STRAP_LO_AG9	THERMTRIP_L	VSS	VSS	VSS	VTT	NC_AG15	MEMDATA[58]
AH	VSS	VSS	VSS	VSS	VSS	STRAP_LO_AH6	VSS	NC_AH8	VSS	STRAP_LO_AH10	VSS	NC_AH12	VSS	VTT	MEMDQS_UP[7]	VSS
AJ	THERMDC	THERMDA	VSS	NC_AJ4	NC_AJ5	NC_AJ6	NC_AJ7	NC_AJ8	TDI	STRAP_LO_AJ10	VDD	STRAP_HI_AJ12	VSS	VTT	MEMDATA[127]	MEMDATA[59]
AK			NC_AK3	NC_AK4	VDD	NC_AK6	VDD	NC_AK8	VDD	NC_AK10	VDD	NC_AK12	VSS	VTT	MEMDATA[122]	VDDIO
AL			NC_AL3	NC_AL4	NC_AL5	NC_AL6	NC_AL7	NC_AL8	NC_AL9	NC_AL10	NC_AL11	NC_AL12	VSS	VTT_AL14	MEMDATA[123]	MEMDATA[126]
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Figure 3. Micro PGA Top View, Left Side

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
MEMDQS_UP[0]	MEMDATA[67]	MEMDATA[72]	MEMDATA[77]	MEMDQS_UP[1]	MEMCLK_1H_H[1]	MEMCLK_1H_L[1]	MEMDATA[74]	MEMDATA[75]	MEMADDB[12]	MEMDATA[80]	MEMDQS_UP[2]	MEMADDB[11]			A
MEMDATA[70]	VDDIO	MEMDATA[76]	VDDIO	MEMDM_UP[1]	VDDIO	MEMDATA[78]	VDDIO	MEMCKEC	VDDIO	MEMDATA[81]	VDDIO	MEMDM_UP[2]	VDDIO		B
MEMDATA[66]	MEMDATA[2]	MEMDATA[73]	MEMDATA[13]	MEMCLK_2H_H[1]	NC_C22	MEMDATA[79]	MEMDATA[10]	MEMCKED	MEMADDA[12]	MEMDATA[85]	NC_C28	MEMADDB[9]	MEMDATA[82]	MEMDATA[86]	C
MEMDATA[71]	VSS	MEMRESET_L	VSS	MEMCLK_2H_L[1]	VSS	MEMCLK_1L_H[1]	VSS	MEMDATA[84]	VSS	MEMDATA[21]	VSS	NC_D29	VDDIO	MEMADDB[7]	D
MEMDM_LO[0]	MEMDATA[7]	MEMDATA[8]	MEMDQS_LO[1]	NC_E21	NC_E22	MEMCLK_1L_L[1]	MEMDATA[11]	MEMCKEB	MEMDATA[17]	MEMDQS_LO[2]	MEMADDA[11]	MEMADDB[8]	MEMDATA[87]	MEMDATA[83]	E
MEMDQS_LO[0]	VSS	MEMDATA[12]			VSS	MEMDATA[14]	VSS	MEMDATA[20]	VSS	MEMDM_LO[2]	VSS	MEMADDA[9]	VDDIO	MEMADDB[5]	F
MEMDATA[6]	MEMDATA[3]	MEMDATA[9]	MEMDM_LO[1]	MEMCLK_2L_H[1]	MEMCLK_2L_L[1]	MEMDATA[15]	MEMCKEA	MEMDATA[16]	MEMDATA[18]	MEMDATA[22]	MEMADDA[7]	MEMADDB[6]	MEMDATA[88]	MEMDATA[92]	G
VSS	VDD	VSS	VDDIO	VSS	VDDIO	VSS	VDDIO	MEMADDA[8]	VSS	MEMDATA[23]	VSS	MEMDATA[19]	VDDIO	MEMDATA[93]	H
VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	VSS	MEMADDA[5]	MEMADDA[6]	MEMDATA[24]	MEMDATA[89]	MEMDQS_UP[3]	MEMDM_UP[3]	MEMADDB[4]	J
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	MEMDATA[28]	VSS	MEMDATA[29]	VSS	MEMDATA[25]	VDDIO	MEMADDB[3]	K
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	MEMDQS_LO[3]	MEMDM_LO[3]	MEMADDA[4]	MEMADDA[3]	MEMDATA[90]	MEMDATA[94]	MEMDATA[91]	L
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	MEMDATA[30]	VSS	MEMDATA[26]	VSS	MEMDATA[27]	VDDIO	MEMDATA[95]	M
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	MEMDATA[31]	MEMADDA[2]	NC_N27	MEMADDB[2]	MEMCHECK[12]	MEMADDB[1]	MEMCHECK[13]	N
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	MEMADDA[1]	VSS	MEMCHECK[5]	VSS	MEMCHECK[0]	VDDIO	MEMCHECK[8]	P
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	MEMCHECK[4]	MEMCLK_1L_L[0]	MEMCLK_1L_H[0]	MEMCHECK[1]	MEMCHECK[9]	MEMCLK_1H_L[0]	MEMCLK_1H_H[0]	R
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	NC_T25	VSS	MEMCLK_2L_H[0]	VSS	NC_T29	VDDIO	MEMCLK_2H_H[0]	T
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	MEMADDA[0]	MEMDQS_LO[8]	MEMCLK_2L_L[0]	NC_U28	MEMADDB[0]	MEMDQS_UP[8]	MEMCLK_2H_L[0]	U
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	MEMCHECK[2]	VSS	MEMADDA[10]	VSS	MEMDM_LO[8]	VDDIO	MEMDM_UP[8]	V
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	MEMBANKA[1]	MEMCHECK[3]	MEMCHECK[6]	MEMCHECK[11]	MEMCHECK[14]	MEMADDB[10]	MEMCHECK[10]	W
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIOFB_H	MEMDATA[36]	VSS	MEMDATA[32]	VSS	MEMCHECK[7]	VDDIO	MEMBANKB[1]	Y
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	VDDIOFB_L	MEMDM_LO[4]	MEMDQS_LO[4]	MEMDATA[33]	MEMDATA[37]	MEMDATA[100]	MEMDATA[96]	MEMCHECK[15]	AA
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	MEMDATA[39]	VSS	MEMDATA[38]	VSS	MEMDATA[34]	VDDIO	MEMDATA[101]	AB
VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	VSS	MEMDATA[44]	MEMDATA[35]	MEMBANKA[0]	MEMDATA[98]	MEMDM_UP[4]	MEMDQS_UP[4]	MEMDATA[97]	AC
VSS	VDD	VSS	VDDIO	VSS	VDDIO	VSS	VDDIO	MEMDATA[45]	VSS	MEMRASA_L	VSS	MEMDATA[40]	VDDIO	MEMDATA[102]	AD
MEMDATA[57]	MEMDATA[60]	MEMDATA[50]	MEMDATA[54]	MEMCLK_2L_L[2]	NC_AE22	MEMDATA[53]	MEMDATA[48]	MEMDATA[46]	MEMCS_2L_L[0]	MEMDATA[41]	MEMWEA_L	MEMDATA[99]	MEMBANKB[0]	MEMDATA[103]	AE
MEMDM_LO[7]			VSS	MEMCLK_2L_H[2]	VSS	MEMADDA[13]	VSS	MEMDATA[43]	VSS	MEMCASA_L	VSS	MEMCS_1L_L[0]	VDDIO	MEMDATA[108]	AF
MEMDATA[62]	MEMDATA[61]	MEMDATA[51]	MEMDQS_LO[6]	MEMDM_LO[6]	NC_AG22	MEMCLK_1L_L[2]	MEMDATA[52]	MEMDATA[47]	MEMDQS_LO[5]	MEMCS_2L_L[1]	MEMCS_1L_L[1]	MEMDATA[109]	MEMRASB_L	MEMDATA[104]	AG
MEMDQS_LO[7]	VSS	MEMDATA[119]	VSS	MEMCLK_2H_L[2]	VSS	MEMCLK_1L_H[2]	VSS	MEMDATA[107]	VSS	MEMDM_LO[5]	VSS	NC_AH29	VDDIO	MEMWEB_L	AH
MEMDATA[120]	MEMDATA[56]	MEMDATA[114]	MEMDATA[55]	MEMCLK_2H_H[2]	NC_AJ22	MEMDATA[117]	MEMDATA[49]	MEMDATA[111]	MEMDATA[42]	MEMDQS_UP[5]	NC_AJ28	MEMCS_1H_L[0]	MEMCS_2H_L[0]	MEMDATA[105]	AJ
MEMDATA[121]	VDDIO	MEMDATA[115]	VDDIO	MEMDM_UP[6]	VDDIO	MEMADDB[13]	VDDIO	MEMDATA[112]	VDDIO	MEMDM_UP[5]	VDDIO	MEMCASB_L	VDDIO		AK
MEMDM_UP[7]	MEMDATA[125]	MEMDATA[124]	MEMDQS_UP[6]	MEMDATA[118]	MEMCLK_1H_H[2]	MEMCLK_1H_L[2]	MEMDATA[113]	MEMDATA[116]	MEMDATA[110]	MEMDATA[106]	MEMCS_2H_L[1]	MEMCS_1H_L[1]			AL
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 4. Micro PGA Top View, Right Side

5 Pin Designations

Table 3, beginning on page 32, lists the pins alphabetically by pin name.

Table 3. Pin List by Name

CLKIN_H	A8	L0_CADIN_L[11]	K4	L0_CADOUT_H[9]	AF5
CLKIN_L	B8	L0_CADIN_L[12]	M4	L0_CADOUT_L[0]	AE1
COREFB_H	E5	L0_CADIN_L[13]	P5	L0_CADOUT_L[1]	AE3
COREFB_L	E6	L0_CADIN_L[14]	P4	L0_CADOUT_L[10]	AD3
CORESENSE	E7	L0_CADIN_L[15]	T5	L0_CADOUT_L[11]	AC5
DBRDY	B11	L0_CADIN_L[2]	J2	L0_CADOUT_L[12]	AA5
DBREQ_L	A6	L0_CADIN_L[3]	K1	L0_CADOUT_L[13]	Y3
FBCLKOUT_H	F13	L0_CADIN_L[4]	M1	L0_CADOUT_L[14]	W5
FBCLKOUT_L	E13	L0_CADIN_L[5]	N2	L0_CADOUT_L[15]	V3
L0_CADIN_H[0]	G3	L0_CADIN_L[6]	P1	L0_CADOUT_L[2]	AC1
L0_CADIN_H[1]	G1	L0_CADIN_L[7]	R2	L0_CADOUT_L[3]	AC3
L0_CADIN_H[10]	J5	L0_CADIN_L[8]	H5	L0_CADOUT_L[4]	AA3
L0_CADIN_H[11]	K3	L0_CADIN_L[9]	H4	L0_CADOUT_L[5]	W1
L0_CADIN_H[12]	M3	L0_CADOUT_H[0]	AF1	L0_CADOUT_L[6]	W3
L0_CADIN_H[13]	N5	L0_CADOUT_H[1]	AE2	L0_CADOUT_L[7]	U1
L0_CADIN_H[14]	P3	L0_CADOUT_H[10]	AD4	L0_CADOUT_L[8]	AF3
L0_CADIN_H[15]	R5	L0_CADOUT_H[11]	AD5	L0_CADOUT_L[9]	AE5
L0_CADIN_H[2]	J3	L0_CADOUT_H[12]	AB5	L0_CLKIN_H[0]	L3
L0_CADIN_H[3]	J1	L0_CADOUT_H[13]	Y4	L0_CLKIN_H[1]	L5
L0_CADIN_H[4]	L1	L0_CADOUT_H[14]	Y5	L0_CLKIN_L[0]	L2
L0_CADIN_H[5]	N3	L0_CADOUT_H[15]	V4	L0_CLKIN_L[1]	M5
L0_CADIN_H[6]	N1	L0_CADOUT_H[2]	AD1	L0_CLKOUT_H[0]	AB1
L0_CADIN_H[7]	R3	L0_CADOUT_H[3]	AC2	L0_CLKOUT_H[1]	AB4
L0_CADIN_H[8]	G5	L0_CADOUT_H[4]	AA2	L0_CLKOUT_L[0]	AA1
L0_CADIN_H[9]	H3	L0_CADOUT_H[5]	Y1	L0_CLKOUT_L[1]	AB3
L0_CADIN_L[0]	G2	L0_CADOUT_H[6]	W2	L0_CTLIN_H[0]	R1
L0_CADIN_L[1]	H1	L0_CADOUT_H[7]	V1	L0_CTLIN_L[0]	T1
L0_CADIN_L[10]	K5	L0_CADOUT_H[8]	AF4	L0_CTLOUT_H[0]	U2

Table 3. Pin List by Name

L0_CTLOUT_L[0]	U3	MEMADDB[6]	G29	MEMCKEC	B25
L0_REF0	C1	MEMADDB[7]	D31	MEMCKED	C25
L0_REF1	D1	MEMADDB[8]	E29	MEMCLK_1H_H[0]	R31
LDTSTOP_L	B6	MEMADDB[9]	C29	MEMCLK_1H_H[1]	A22
MEMADDA[0]	U25	MEMBANKA[0]	AC27	MEMCLK_1H_H[2]	AL22
MEMADDA[1]	P25	MEMBANKA[1]	W25	MEMCLK_1H_L[0]	R30
MEMADDA[10]	V27	MEMBANKB[0]	AE30	MEMCLK_1H_L[1]	A23
MEMADDA[11]	E28	MEMBANKB[1]	Y31	MEMCLK_1H_L[2]	AL23
MEMADDA[12]	C26	MEMCASA_L	AF27	MEMCLK_1L_H[0]	R27
MEMADDA[13]	AF23	MEMCASB_L	AK29	MEMCLK_1L_H[1]	D23
MEMADDA[2]	N26	MEMCHECK[0]	P29	MEMCLK_1L_H[2]	AH23
MEMADDA[3]	L28	MEMCHECK[1]	R28	MEMCLK_1L_L[0]	R26
MEMADDA[4]	L27	MEMCHECK[10]	W31	MEMCLK_1L_L[1]	E23
MEMADDA[5]	J25	MEMCHECK[11]	W28	MEMCLK_1L_L[2]	AG23
MEMADDA[6]	J26	MEMCHECK[12]	N29	MEMCLK_2H_H[0]	T31
MEMADDA[7]	G28	MEMCHECK[13]	N31	MEMCLK_2H_H[1]	C21
MEMADDA[8]	H25	MEMCHECK[14]	W29	MEMCLK_2H_H[2]	AJ21
MEMADDA[9]	F29	MEMCHECK[15]	AA31	MEMCLK_2H_L[0]	U31
MEMADDB[0]	U29	MEMCHECK[2]	V25	MEMCLK_2H_L[1]	D21
MEMADDB[1]	N30	MEMCHECK[3]	W26	MEMCLK_2H_L[2]	AH21
MEMADDB[10]	W30	MEMCHECK[4]	R25	MEMCLK_2L_H[0]	T27
MEMADDB[11]	A29	MEMCHECK[5]	P27	MEMCLK_2L_H[1]	G21
MEMADDB[12]	A26	MEMCHECK[6]	W27	MEMCLK_2L_H[2]	AF21
MEMADDB[13]	AK23	MEMCHECK[7]	Y29	MEMCLK_2L_L[0]	U27
MEMADDB[2]	N28	MEMCHECK[8]	P31	MEMCLK_2L_L[1]	G22
MEMADDB[3]	K31	MEMCHECK[9]	R29	MEMCLK_2L_L[2]	AE21
MEMADDB[4]	J31	MEMCKEA	G24	MEMCS_1H_L[0]	AJ29
MEMADDB[5]	F31	MEMCKEB	E25	MEMCS_1H_L[1]	AL29

Table 3. Pin List by Name

MEMCS_1L_L[0]	AF29	MEMDATA[118]	AL21	MEMDATA[29]	K27
MEMCS_1L_L[1]	AG28	MEMDATA[119]	AH19	MEMDATA[3]	G18
MEMCS_2H_L[0]	AJ30	MEMDATA[12]	F19	MEMDATA[30]	M25
MEMCS_2H_L[1]	AL28	MEMDATA[120]	AJ17	MEMDATA[31]	N25
MEMCS_2L_L[0]	AE26	MEMDATA[121]	AK17	MEMDATA[32]	Y27
MEMCS_2L_L[1]	AG27	MEMDATA[122]	AK15	MEMDATA[33]	AA27
MEMDATA[0]	C16	MEMDATA[123]	AL15	MEMDATA[34]	AB29
MEMDATA[1]	G16	MEMDATA[124]	AL19	MEMDATA[35]	AC26
MEMDATA[10]	C24	MEMDATA[125]	AL18	MEMDATA[36]	Y25
MEMDATA[100]	AA29	MEMDATA[126]	AL16	MEMDATA[37]	AA28
MEMDATA[101]	AB31	MEMDATA[127]	AJ15	MEMDATA[38]	AB27
MEMDATA[102]	AD31	MEMDATA[13]	C20	MEMDATA[39]	AB25
MEMDATA[103]	AE31	MEMDATA[14]	F23	MEMDATA[4]	E15
MEMDATA[104]	AG31	MEMDATA[15]	G23	MEMDATA[40]	AD29
MEMDATA[105]	AJ31	MEMDATA[16]	G25	MEMDATA[41]	AE27
MEMDATA[106]	AL27	MEMDATA[17]	E26	MEMDATA[42]	AJ26
MEMDATA[107]	AH25	MEMDATA[18]	G26	MEMDATA[43]	AF25
MEMDATA[108]	AF31	MEMDATA[19]	H29	MEMDATA[44]	AC25
MEMDATA[109]	AG29	MEMDATA[2]	C18	MEMDATA[45]	AD25
MEMDATA[11]	E24	MEMDATA[20]	F25	MEMDATA[46]	AE25
MEMDATA[110]	AL26	MEMDATA[21]	D27	MEMDATA[47]	AG25
MEMDATA[111]	AJ25	MEMDATA[22]	G27	MEMDATA[48]	AE24
MEMDATA[112]	AK25	MEMDATA[23]	H27	MEMDATA[49]	AJ24
MEMDATA[113]	AL24	MEMDATA[24]	J27	MEMDATA[5]	E16
MEMDATA[114]	AJ19	MEMDATA[25]	K29	MEMDATA[50]	AE19
MEMDATA[115]	AK19	MEMDATA[26]	M27	MEMDATA[51]	AG19
MEMDATA[116]	AL25	MEMDATA[27]	M29	MEMDATA[52]	AG24
MEMDATA[117]	AJ23	MEMDATA[28]	K25	MEMDATA[53]	AE23

Table 3. Pin List by Name

MEMDATA[54]	AE20	MEMDATA[8]	E19	MEMDM_LO[6]	AG21
MEMDATA[55]	AJ20	MEMDATA[80]	A27	MEMDM_LO[7]	AF17
MEMDATA[56]	AJ18	MEMDATA[81]	B27	MEMDM_LO[8]	V29
MEMDATA[57]	AE17	MEMDATA[82]	C30	MEMDM_UP[0]	A16
MEMDATA[58]	AG16	MEMDATA[83]	E31	MEMDM_UP[1]	B21
MEMDATA[59]	AJ16	MEMDATA[84]	D25	MEMDM_UP[2]	B29
MEMDATA[6]	G17	MEMDATA[85]	C27	MEMDM_UP[3]	J30
MEMDATA[60]	AE18	MEMDATA[86]	C31	MEMDM_UP[4]	AC29
MEMDATA[61]	AG18	MEMDATA[87]	E30	MEMDM_UP[5]	AK27
MEMDATA[62]	AG17	MEMDATA[88]	G30	MEMDM_UP[6]	AK21
MEMDATA[63]	AE16	MEMDATA[89]	J28	MEMDM_UP[7]	AL17
MEMDATA[64]	B15	MEMDATA[9]	G19	MEMDM_UP[8]	V31
MEMDATA[65]	D15	MEMDATA[90]	L29	MEMDQS_LO[0]	F17
MEMDATA[66]	C17	MEMDATA[91]	L31	MEMDQS_LO[1]	E20
MEMDATA[67]	A18	MEMDATA[92]	G31	MEMDQS_LO[2]	E27
MEMDATA[68]	A15	MEMDATA[93]	H31	MEMDQS_LO[3]	L25
MEMDATA[69]	C15	MEMDATA[94]	L30	MEMDQS_LO[4]	AA26
MEMDATA[7]	E18	MEMDATA[95]	M31	MEMDQS_LO[5]	AG26
MEMDATA[70]	B17	MEMDATA[96]	AA30	MEMDQS_LO[6]	AG20
MEMDATA[71]	D17	MEMDATA[97]	AC31	MEMDQS_LO[7]	AH17
MEMDATA[72]	A19	MEMDATA[98]	AC28	MEMDQS_LO[8]	U26
MEMDATA[73]	C19	MEMDATA[99]	AE29	MEMDQS_UP[0]	A17
MEMDATA[74]	A24	MEMDM_LO[0]	E17	MEMDQS_UP[1]	A21
MEMDATA[75]	A25	MEMDM_LO[1]	G20	MEMDQS_UP[2]	A28
MEMDATA[76]	B19	MEMDM_LO[2]	F27	MEMDQS_UP[3]	J29
MEMDATA[77]	A20	MEMDM_LO[3]	L26	MEMDQS_UP[4]	AC30
MEMDATA[78]	B23	MEMDM_LO[4]	AA25	MEMDQS_UP[5]	AJ27
MEMDATA[79]	C23	MEMDM_LO[5]	AH27	MEMDQS_UP[6]	AL20

Table 3. Pin List by Name

MEMDQS_UP[7]	AH15	NC_U28	U28	NC_D4	D4
MEMDQS_UP[8]	U30	NC_C28	C28	NC_A4	A4
MEMRASA_L	AD27	NC_E21	E21	NC_E9	E9
MEMRASB_L	AG30	NC_AG22	AG22	NC_C13	C13
MEMRESET_L	D19	NC_AJ28	AJ28	NC_C7	C7
MEMVREF	F15	NC_AL9	AL9	NC_AL8	AL8
MEMWEA_L	AE28	NC_AK6	AK6	NC_AL7	AL7
MEMWEB_L	AH31	NC_AK8	AK8	NC_V5	V5
MEMZN	AF15	NC_AK10	AK10	NC_U5	U5
MEMZP	AE15	NC_AK12	AK12	PWROK	E8
NC_AH12	AH12	NC_D11	D11	RESET_L	F8
NC_D12	D12	NC_T25	T25	STRAP_LO_AH6	AH6
NC_AJ5	AJ5	NC_AL3	AL3	STRAP_LO_AG9	AG9
NC_AJ7	AJ7	NC_AK3	AK3	STRAP_LO_AF10	AF10
NC_AK4	AK4	NC_T29	T29	STRAP_LO_C10	C10
NC_AL5	AL5	NC_G15	G15	STRAP_LO_B13	B13
NC_AL11	AL11	NC_D8	D8	STRAP_LO_F11	F11
NC_E22	E22	NC_AH8	AH8	STRAP_LO_T4	T4
NC_AJ6	AJ6	NC_D29	D29	STRAP_LO_AJ10	AJ10
NC_AJ8	AJ8	NC_AH29	AH29	STRAP_LO_AH10	AH10
NC_AL4	AL4	NC_AJ4	AJ4	STRAP_HI_AF12	AF12
NC_AL6	AL6	NC_AG15	AG15	STRAP_HI__E11	E11
NC_AL10	AL10	NC_C11	C11	STRAP_HI_T3	T3
NC_AL12	AL12	NC_C5	C5	STRAP_HI_AJ12	AJ12
NC_N27	N27	NC_A5	A5	TCK	AG7
NC_AJ22	AJ22	NC_C6	C6	TDI	AJ9
NC_C22	C22	NC_C4	C4	TDO	AG8
NC_AE22	AE22	NC_B4	B4	THERMDA	AJ2

Table 3. Pin List by Name

THERMDC	AJ1	VDD	G13	VDD	M8
THERMTRIP_L	AG10	VDD	V6	VDD	M12
TMS	AG6	VDD	AJ11	VDD	K8
TRST_L	AF8	VDD	AC9	VDD	P14
VDD	B5	VDD	H16	VDD	U17
VDD	B12	VDD	K16	VDD	T20
VDD	AK5	VDD	P16	VDD	V20
VDD	AK7	VDD	T16	VDD	U19
VDD	AK9	VDD	V8	VDD	R21
VDD	AK11	VDD	P20	VDD	W21
VDD	J4	VDD	Y20	VDD	AA19
VDD	N4	VDD	W19	VDD	AA21
VDD	H2	VDD	L17	VDD	AC19
VDD	K6	VDD	T18	VDD	T8
VDD	P6	VDD	M16	VDD	K20
VDD	T6	VDD	J15	VDD	K18
VDD	M2	VDD	R15	VDD	H12
VDD	H6	VDD	R17	VDD	H18
VDD	AD6	VDD	J17	VDD	K14
VDD	AB6	VDD	V16	VDD	V10
VDD	Y6	VDD	P18	VDD	H10
VDD	AD2	VDD	J19	VDD	P10
VDD	Y2	VDD	V18	VDD	P8
VDD	AE4	VDD	M20	VDD	P12
VDD	AA4	VDD	L19	VDD	N19
VDD	M6	VDD	M18	VDD	N17
VDD	T2	VDD	K12	VDD	T12
VDD	U4	VDD	K10	VDD	N21

Table 3. Pin List by Name

VDD	R19	VDD	AB12	VDD	U11
VDD	V12	VDD	AC11	VDD	W15
VDD	T14	VDD	AC13	VDD	W17
VDD	V14	VDD	AD8	VDD	Y14
VDD	U21	VDD	AD10	VDD	Y16
VDD	AB20	VDD	AD12	VDD	Y18
VDD	M14	VDD	AE7	VDD	AA13
VDD	N15	VDD	AE9	VDD	AA15
VDD	L21	VDD	AE11	VDD	AA17
VDD	L15	VDD	L9	VDD	AB14
VDD	M10	VDD	L11	VDD	AB16
VDD	H14	VDD	N9	VDD	AB18
VDD	T10	VDD	N11	VDD	AC15
VDD	H8	VDD	U13	VDD	AC17
VDD	B10	VDD	G11	VDD	AD14
VDD	D10	VDD	L13	VDD	AD16
VDD	W7	VDD	N13	VDD	AD18
VDD	W9	VDD	U15	VDD	J7
VDD	W11	VDD	G7	VDD	L7
VDD	W13	VDD	G9	VDD	N7
VDD	Y8	VDD	J9	VDD	R7
VDD	Y10	VDD	J11	VDDA	A3
VDD	Y12	VDD	J13	VDDA	B3
VDD	AA7	VDD	R9	VDDA	C3
VDD	AA9	VDD	R11	VDDIO	T30
VDD	AA11	VDD	R13	VDDIO	AH30
VDD	AB8	VDD	U7	VDDIO	D30
VDD	AB10	VDD	U9	VDDIO	F30

Table 3. Pin List by Name

VDDIO	AK24	VDDIO	P22	VDDIOSENSE	AE13
VDDIO	AK30	VDDIO	R23	VID[0]	A10
VDDIO	P30	VDDIO	V24	VID[1]	A11
VDDIO	Y30	VDDIO	AD24	VID[2]	C12
VDDIO	AF30	VDDIO	AB24	VID[3]	A12
VDDIO	AK26	VDDIO	T22	VID[4]	A13
VDDIO	AK20	VDDIO	AD20	VLDT_A	F2
VDDIO	AK18	VDDIO	AB22	VLDT_A	F1
VDDIO	AK16	VDDIO	V22	VLDT_A	E1
VDDIO	H30	VDDIO	U23	VLDT_A	E2
VDDIO	K30	VDDIO	AD22	VLDT_B	AG2
VDDIO	M30	VDDIO	L23	VLDT_B	AG1
VDDIO	AB30	VDDIO	H22	VLDT_B	AG3
VDDIO	AD30	VDDIO	M22	VLDT_B	AG4
VDDIO	B16	VDDIO	W23	VSS	G12
VDDIO	B18	VDDIO	AA23	VSS	AG12
VDDIO	B26	VDDIO	AC21	VSS	D5
VDDIO	B20	VDDIO	AC23	VSS	E10
VDDIO	B24	VDDIO	Y22	VSS	E12
VDDIO	B28	VDDIO	J21	VSS	F12
VDDIO	V30	VDDIO	N23	VSS	A9
VDDIO	B22	VDDIO	H20	VSS	B9
VDDIO	B30	VDDIO	P24	VSS	A7
VDDIO	AK28	VDDIO	H24	VSS	AH13
VDDIO	AK22	VDDIO	K24	VSS	C8
VDDIO	J23	VDDIO	T24	VSS	F14
VDDIO	K22	VDDIOFB_H	Y24	VSS	D13
VDDIO	M24	VDDIOFB_L	AA24	VSS	AK13

Table 3. Pin List by Name

VSS	T26	VSS	V28	VSS	AD26
VSS	AL13	VSS	AF24	VSS	D16
VSS	D9	VSS	H26	VSS	D18
VSS	AH9	VSS	AF28	VSS	D26
VSS	G4	VSS	V26	VSS	F18
VSS	J6	VSS	P28	VSS	F28
VSS	N6	VSS	AH22	VSS	AH28
VSS	R6	VSS	D22	VSS	AH16
VSS	R4	VSS	D24	VSS	AH18
VSS	G6	VSS	AH24	VSS	AD28
VSS	K2	VSS	T28	VSS	D20
VSS	P2	VSS	AF22	VSS	F16
VSS	AF2	VSS	AH1	VSS	AF16
VSS	V2	VSS	AH26	VSS	AG13
VSS	AF6	VSS	AH20	VSS	F9
VSS	AC6	VSS	F24	VSS	AH7
VSS	AA6	VSS	F26	VSS	AF11
VSS	W6	VSS	D28	VSS	U6
VSS	AC4	VSS	H28	VSS	AH11
VSS	W4	VSS	M28	VSS	AJ13
VSS	AE6	VSS	K26	VSS	AJ3
VSS	L4	VSS	K28	VSS	AG11
VSS	L6	VSS	M26	VSS	AF9
VSS	AB2	VSS	Y28	VSS	T15
VSS	C2	VSS	Y26	VSS	V13
VSS	D2	VSS	AB28	VSS	Y13
VSS	B7	VSS	AB26	VSS	AD13
VSS	P26	VSS	AF26	VSS	AB13

Table 3. Pin List by Name

VSS	AB21	VSS	Y21	VSS	K13
VSS	Y19	VSS	V11	VSS	AA14
VSS	T19	VSS	AD19	VSS	AB15
VSS	P19	VSS	H19	VSS	AC14
VSS	K15	VSS	T9	VSS	AD15
VSS	M17	VSS	K11	VSS	L14
VSS	P15	VSS	H9	VSS	L16
VSS	T17	VSS	K9	VSS	L18
VSS	H17	VSS	H11	VSS	L20
VSS	V15	VSS	N8	VSS	L22
VSS	P9	VSS	R8	VSS	N14
VSS	V9	VSS	T11	VSS	N16
VSS	M21	VSS	N10	VSS	N18
VSS	K19	VSS	R10	VSS	N20
VSS	L12	VSS	N12	VSS	N22
VSS	M19	VSS	P17	VSS	W14
VSS	K17	VSS	P21	VSS	W16
VSS	M15	VSS	U10	VSS	W18
VSS	J12	VSS	H15	VSS	Y15
VSS	U12	VSS	G10	VSS	Y17
VSS	L10	VSS	T21	VSS	AA16
VSS	L8	VSS	K21	VSS	AA18
VSS	M11	VSS	J8	VSS	AB17
VSS	M9	VSS	AB19	VSS	AC16
VSS	V17	VSS	J10	VSS	AC18
VSS	V19	VSS	R12	VSS	AD17
VSS	P11	VSS	U8	VSS	H13
VSS	V21	VSS	G8	VSS	T13

Table 3. Pin List by Name

VSS	M13	VSS	AA8	VSS	H21
VSS	U14	VSS	AA10	VSS	K23
VSS	G14	VSS	AA12	VSS	M23
VSS	H7	VSS	AA20	VSS	H23
VSS	J14	VSS	AA22	VSS	AB23
VSS	J16	VSS	AB7	VSS	Y23
VSS	J18	VSS	AB9	VSS	N24
VSS	J20	VSS	AB11	VSS	U24
VSS	P13	VSS	AC10	VSS	J22
VSS	R14	VSS	AC12	VSS	J24
VSS	R16	VSS	AC20	VSS	R24
VSS	R18	VSS	AD7	VSS	AC22
VSS	R20	VSS	AD9	VSS	AE14
VSS	R22	VSS	AD11	VSS	E3
VSS	T7	VSS	AE8	VSS	AG5
VSS	U16	VSS	AE10	VSS	AF20
VSS	U18	VSS	AE12	VSS	F22
VSS	U20	VSS	K7	VSS	F5
VSS	U22	VSS	M7	VSS	AH2
VSS	V7	VSS	P7	VSS	F10
VSS	W8	VSS	L24	VSS	C9
VSS	W10	VSS	AC24	VSS	D6
VSS	W12	VSS	W24	VSS	AH4
VSS	W20	VSS	V23	VSS	F6
VSS	W22	VSS	T23	VSS	D3
VSS	Y7	VSS	P23	VSS	D7
VSS	Y9	VSS	AD23	VSS	E4
VSS	Y11	VSS	AD21	VSS	F7

Table 3. Pin List by Name

VSS	AF7
VSS	AH3
VSS	AH5
VSS	AF14
VTT	E14
VTT	AG14
VTT	B14
VTT	C14
VTT	AJ14
VTT	D14
VTT	AH14
VTT	AK14
VTT_A14	A14
VTT_AL14	AL14
VTT_SENSE	AF13

6 Pin Descriptions

Table 4 describes the terms used in the pin description tables found in this chapter. The pins are organized within the following functional groups:

- HyperTransport™ technology interface
- DDR SDRAM memory interface
- Miscellaneous pins, including clock, JTAG, and debug pins

All pins are described in the tables beginning on page 46.

Table 4. Pin Description Table Definitions

Pin Types		Applicable Section in Electrical Chapter
I-HT	Input, HyperTransport™ Technology, Differential	"HyperTransport™ Technology Interface" on page 54
O-HT	Output, HyperTransport™ Technology, Differential	"HyperTransport™ Technology Interface" on page 54
B-IOS	Bidirectional, VDDIO[1], Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 58
I-IOS	Input, VDDIO[1], Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 58
I-IOD	Input, VDDIO[1], Differential	"Clock Pins" on page 70
O-IOD	Output, VDDIO[1], Differential	"Clock Pins" on page 70
O-IOS	Output, VDDIO[1], Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 58
O-IO-OD	Output, VDDIO[1], Open Drain	"DDR SDRAM and Miscellaneous Pins" on page 58
A	Analog	"Power Supplies" on page 79
S	Supply Voltage	"Power Supplies" on page 79
VREF	Voltage Reference	"DDR SDRAM and Miscellaneous Pins" on page 58

Notes:

1. *Refer to Table 30, "Combined AC and DC Operating Conditions for Power Supplies," on page 79 for VDDIO voltage specifications.*

6.1 HyperTransport™ Technology Pins

Table 5. HyperTransport™ Technology Pin Descriptions

Signal Name	Type	Description
L0_CLKIN_H/L[1:0]	I-HT	Link 0 Clock Input
L0_CTLIN_H/L[1:0]	I-HT	Link 0 Control Input[2]
L0_CADIN_H/L[15:0]	I-HT	Link 0 Command/Address/Data Input
L0_CLKOUT_H/L[1:0]	O-HT	Link 0 Clock Outputs
L0_CTLOUT_H/L[1:0]	O-HT	Link 0 Control Output
L0_CADOUT_H/L[15:0]	O-HT	Link 0 Command/Address/Data Outputs
L0_REF1	A	Compensation Resistor to VLDT[1]
L0_REF0	A	Compensation Resistor to VSS[1]

Notes:

1. *These pins are used in an alternating fashion to compensate R_{TT} by internal comparison to 3/4 VLDT and 1/4 VLDT and compensate R_{ON} by comparison to each other around 1/2 VLDT. For the proper resistor value, refer to the AMD Athlon™ 64 939 Motherboard Design Guide, order# 30474.*
2. *The unused L0_CTLIN_H/L[1] pins must be properly terminated such that the true pin is pulled High and the complement is pulled Low. Refer to the AMD Athlon™ 64 939 Motherboard Design Guide, order# 30474, for details.*

6.2 DDR SDRAM Memory Interface Pins

Table 6. DDR SDRAM Memory Interface Pin Descriptions

Signal Name	Type	Description
MEMCLK_1L_H/L[2:0]	O-IOD	Differential clocks to DIMM 1 lower half
MEMCLK_1H_H/L[2:0]	O-IOD	Differential clocks to DIMM 1 upper half
MEMCLK_2L_H/L[2:0]	O-IOD	Differential clocks to DIMM 2 lower half
MEMCLK_2H_H/L[2:0]	O-IOD	Differential clocks to DIMM 2 upper half
MEMCKE[D:A]	O-IOS	Clock Enables to DIMMs. Used to gate clocks for power management functionality
MEMDQS_LO[8:0]	B-IOS	Data Strobes to lower half of data bus, synchronous with MEMDATA and MEMCHECK during DRAM read and writes
MEMDQS_HI[8:0]	B-IOS	Data Strobes to upper half of data bus, synchronous with MEMDATA and MEMCHECK during DRAM read and writes
MEMDM_LO[8:0]	B-IOS	Data Mask pins to lower half of data bus
MEMDM_HI[8:0]	B-IOS	Data Mask pins to upper half of data bus
MEMDATA[128:0]	B-IOS	DRAM Interface Data Bus
MEMCHECK[15:0]	B-IOS	DRAM Interface ECC Check Bits
MEMCS_1L_L[1:0]	O-IOS	DRAM Chip Selects to lower half of data bus
MEMCS_1H_L[1:0]	O-IOS	DRAM Chip Selects to upper half of data bus
MEMCS_2L_L[1:0]	O-IOS	DRAM Chip Selects to lower half of data bus
MEMCS_2H_L[1:0]	O-IOS	DRAM Chip Selects to upper half of data bus
MEMRASA_L MEMRASB_L	O-IOS	DRAM Row Address Select. MEMRASA_L and MEMRASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.
MEMCASA_L MEMCASB_L	O-IOS	DRAM Column Address Select. MEMCASA_L and MEMCASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.
MEMWEA_L MEMWEB_L	O-IOS	DRAM Write Enable. MEMWEA_L and MEMWEB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.
MEMADDA[13:0] MEMADDB[13:0]	O-IOS	DRAM Column/Row Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes, the two copies are inverted from each other (except A[10] which is used for auto-precharge) to minimize switching noise. The signals are inverted only when the bus is used to carry address information.

Table 6. DDR SDRAM Memory Interface Pin Descriptions (Continued)

Signal Name	Type	Description
MEMBANKA[1:0] MEMBANKB[1:0]	O-IOS	DRAM Bank Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes the two copies are inverted from each other to minimize switching noise. The signals are inverted only when the bus is used to carry address information.
MEMVREF	VREF	DRAM Interface Voltage Reference[1]
MEMZP	A	Compensation Resistor tied to VSS[1]
MEMZN	A	Compensation Resistor tied to 2.5 V[1]

Notes:

1. *For connection details and proper resistor values, see the AMD Athlon™ 64 939 Motherboard Design Guide, order# 30474.*

6.3 Miscellaneous Pins

For connection details for all of the pins in this section, please see the *AMD Athlon™ 64 939 Motherboard Design Guide,* order# 30474.

Table 7. Clock Pin Descriptions

Signal Name	Type	Description
CLKIN_H/L	I-IOD	200-MHz PLL Reference Clock
FBCLKOUT_H/L	O-IOD	Core Clock PLL 200-MHz Feedback Clock

Table 8. Miscellaneous Pin Descriptions

Signal Name	Type	Description
RESET_L	I-IOS	System Reset
PWROK	I-IOS	Indicates that voltages and clocks have reached specified operation
LDTSTOP_L	I-IOS	HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport™ link width and frequency.
VID[4:0]	O-IOS	Voltage ID to the regulator[1]
THERMDA	A	Anode (+) of the thermal diode
THERMDC	A	Cathode (–) of the thermal diode
THERMTRIP_L	O-IO-OD	Thermal Sensor Trip output, asserted at nominal temperature of 125°C.
COREFB_H/L	A	Differential feedback for VDD Power Supply
VDDIOFB_H/L	A	Differential feedback for VDDIO Power Supply
CORE_SENSE	A	VDD voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VTT_SENSE	A	VTT voltage monitor pin
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDD	S	Core power supply
VDDIO	S	DDR SDRAM I/O ring power supply
VLDT_A VLDT_B	S	HyperTransport™ I/O ring power supply
VTT	S	VTT regulator voltage
VSS	S	Ground

Notes:
1. *Refer to the BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors, order# 26094, for VID encoding values.*

Table 9. JTAG Pin Descriptions

Signal Name	Type	Description
TCK	I-IOS	JTAG Clock
TMS	I-IOS	JTAG Mode Select
TRST_L	I-IOS	JTAG Reset
TDI	I-IOS	JTAG Data Input
TDO	O-IOS	JTAG Data Output

Table 10. Debug Pin Descriptions

Signal Name	Type	Description
DBREQ_L	I-IOS	Debug Request
DBRDY	O-IOS	Debug Ready

6.4 Pin States at Reset

The default pin states are listed in Table 11 on page 51. Default pin states are listed for all output and bidirectional pins in the power-on reset state (reset), as well as the ACPI S1 and S3 power-management states.

Table 11. Reset Pin State

Pin Name	Reset State	S1 State	S3 State	Comments
L0_CLKOUT*	T	Z	Z	Tristated in S1 only if programmed to do so.
L0_CTLOUT*	0	Z	Z	Tristated in S1 only if programmed to do so.
L0_CADOUT*	1	Z	Z	Tristated in S1 only if programmed to do so.
MEMCLK*	Z	Z	Z	
MEMDQS*	Z	Z	Z	
MEMDM*	Z	Z	Z	
MEMCKE*	0	0	0	In S3, MEMCKE* is forced to a logic Low.
MEMDATA*	Z	Z	Z	
MEMCHECK*	Z	Z	Z	
MEMCS_L*	1	Z	Z	
MEMRAS_L	1	Z	Z	
MEMCAS_L	1	Z	Z	
MEMWE_L	1	Z	Z	
MEMADDA*	0	Z	Z	
MEMADDB*	1	Z	Z	MEMADDB* pins are opposite polarity to reduce switching noise.
MEMBANKA*	0	Z	Z	
MEMBANKB*	1	Z	Z	MEMBANKB* pins are opposite polarity to reduce switching noise.
MEMZN	1	1	1	
MEMZP	0	0	0	
FBCLKOUT*	T	T	Z	
TDO	X	X	Z	
DBRDY	0	0	Z	
VID[4:0]	X	X	X	
THERMTRIP_L	Z	X	Z	

Notes:
For differential inputs, "0" and "1" refer to the high-end differential output. Low-end differential outputs are inverted.
Definitions of pin states: X = either logic 1 or 0; Z = tristated; T = toggling between 0 and 1.

7 Electrical Data

7.1 Absolute Maximum Ratings

Stresses greater than those listed in Table 12 may cause permanent damage to the device and motherboard. Systems using this device must be designed to ensure that these parameters are not violated. Violation of these ratings will void the product warranty. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12. Absolute Maximum Ratings

Characteristic	Range
Storage temperature	–55°C to 85°C
VLDT supply voltage relative to VSS	–0.3 V to 1.5 V
VDD supply voltage relative to VSS	–0.3 V to 1.65 V
VTT supply voltage relative to VSS	–0.3 V to 1.65 V
VDDIO supply voltage relative to VSS	–1 V to 2.9 V
VDDA supply voltage relative to VSS	–0.3 V to 3.0 V
MEMVREF input voltage relative to VSS	–1 V to 2.9 V
Input voltage relative to VSS for HyperTransport™ technology interface	–0.3 V to 1.5 V
Differential input voltage for HyperTransport™ technology interface	–1.5 V to 1.5 V
Input voltage relative to VSS for DDR SDRAM memory interface and Miscellaneous pins	–1 V to 2.9V

Refer to the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet,* order# 30430, for maximum case temperature specifications.

7.2 HyperTransport™ Technology Interface

7.2.1 Operating Conditions

Table 13. DC Operating Conditions for HyperTransport™ Technology Interface

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OD}	Output Differential Voltage	mV	495	600	715	1, 2
V_{OCM}	Output Common Mode Voltage	mV	495	600	715	1, 2
V_{ID}	Input Differential Voltage	mV	100	600	1000	1, 2
V_{ICM}	Input Common Mode Voltage	mV	440	600	780	1, 2
DeltaV_{OD}	Change in V_{OD} from 0 to 1 State	mV	–15	0	15	1
DeltaV_{OCM}	Change in V_{OCM} from 0 to 1 State	mV	–15	0	15	1
DeltaV_{ID}	Change in V_{ID} from 0 to 1 State	mV	–15	0	15	1
DeltaV_{ICM}	Change in V_{ICM} from 0 to 1 State	mV	–15	0	15	1
I_I	Input Leakage Current	µA	–500		500	
I_{OZ}	Output Tristate Leakage Current	mA	-1		1	
R_{TT}	Input Differential Impedance	ohm	90	100	110	
R_{ON}	Output Driver Impedance	ohm	45	50	55	
DeltaR_{ON}	Change in R_{ON} driving 0=>1 or 1=>0	%	0		5	

Notes:

1. *Measured by comparing each signal voltage with respect to ground.*
2. *Measured at <100 MHz, considered slow enough to attain both 0 and 1 logic state voltage levels without AC transients on signals and supplies.*

Table 14. AC Operating Conditions for HyperTransport™ Technology Interface

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OD}	Output Differential Voltage	mV	400	600	820	1
V_{OCM}	Output Common Mode Voltage	mV	440	600	780	1
V_{ID}	Input Differential Voltage	mV	200	600	900	1, 3
V_{ICMAC}	Peak-to-peak Magnitude of Input Common Mode Voltage	mV			350	1, 3
DeltaV_{OD}	Change in V_{OD} from 0 to 1 State	mV	–75		75	1
DeltaV_{OCM}	Change in V_{OCM} from 0 to 1 State	mV	–50		50	1
DeltaV_{ID}	Change in V_{ID} from 0 to 1 State	mV	–125		125	1
T_R	Input Rising Slew Rate	V/ns	2.0		8.0	1, 2, 3
T_F	Input Falling Slew Rate	V/ns	2.0		8.0	1, 2, 3
T_{OR}	Output Rising Slew Rate	V/ns	2.5		8.0	4
T_{OF}	Output Falling Slew Rate	V/ns	2.5		8.0	4
C_{IN}	Input Pad Capacitance	pF			2	5
C_{OUT}	Output Pad Capacitance	pF			3	5
C_{DELTA}	C_{IN} Pad Capacitance Range Across Group	pF			0.5	

Notes:

1. *Measured by comparing each signal voltage with respect to ground.*
2. *Measured differentially between +/-100 mV.*
3. *Measured or simulated at the receive die pad.*
4. *Output slew rates are measured differentially between +/-200 mV.*
5. *C_{IN} and C_{OUT} are measured with a Time Domain Reflectometer (TDR) set to a low repeat rate or equivalent measurement technique.*

Table 15. HyperTransport™ Technology Interface Timing Characteristics

Symbol	Parameter	Unit	Min	Typ	Max	Notes
T_{CADV}	Output CAD Valid, 200 MHz	pS	695		1805	1, 5
	Output CAD Valid, 400 MHz	pS	345		905	1, 5
	Output CAD Valid, 600 MHz	pS	234		600	1, 5
	Output CAD Valid, 800 MHz	pS	166		459	1, 5
	Output CAD Valid, 1000 MHz	pS	183			1, 4, 5
T_{CADVRS}	Receiver CADIN Valid Time to CLKIN, 200 MHz	pS	460			1, 3
	Receiver CADIN Valid Time to CLKIN, 400 MHz	pS	225			1, 3
	Receiver CADIN Valid Time to CLKIN, 600 MHz	pS	166			1, 3
	Receiver CADIN Valid Time to CLKIN, 800 MHz	pS	120			1, 3
	Receiver CADIN Valid Time to CLKIN, 1000 MHz	pS	92			1, 3
T_{CADVRH}	Receiver CADIN Valid Time from CLKIN, 200 MHz	pS	460			1, 3
	Receiver CADIN Valid Time from CLKIN, 400 MHz	pS	225			1, 3
	Receiver CADIN Valid Time from CLKIN, 600 MHz	pS	166			1, 3
	Receiver CADIN Valid Time from CLKIN, 800 MHz	pS	120			1, 3
	Receiver CADIN Valid Time from CLKIN, 1000 MHz	pS	105			1, 3
TPHERR	Accumulated Phase Error, CLKIN_H/L to L0_CLKOUT_H/L[1:0]	pS	0		5000	
PLL_Lock	PLL Lock Time During FID_Change	µs			2	
T_{SU}	Device Setup Time, 200 MHz	pS			250	1, 2
	Device Setup Time, 400 MHz	pS			175	1, 2
	Device Setup Time, 600 MHz	pS			138	1, 2
	Device Setup Time, 800 MHz	pS			110	1, 2
	Device Setup Time, 1000 MHz	pS			85	1, 2

Table 15. HyperTransport™ Technology Interface Timing Characteristics

Symbol	Parameter	Unit	Min	Typ	Max	Notes
T_{HLD}	Device Hold Time, 200 MHz	pS			250	1, 2
	Device Hold Time, 400 MHz	pS			175	1, 2
	Device Hold Time, 600 MHz	pS			138	1, 2
	Device Hold Time, 800 MHz	pS			110	1, 2
	Device Hold Time, 1000 MHz	pS			98	1, 2

Notes:

1. *All timing measurement points are at the zero crossing points of differential pairs.*
2. *Measured or simulated at the receive die pad.*
3. *Measured at the receiver pins.*
4. *T_{CADV} of 183ps for 1000 MHz operation implies a maximum TX CAD to CLK skew of 67ps at the device pins. Refer to the HyperTransport™ I/O Link Specification for further details.*
5. *Measured at the transmitter pins into the ideal test load described in the HyperTransport™ I/O Link Specification.*

7.2.2 Reference Information

Table 16. Internal Termination for HyperTransport™ Technology Interface

Pin	Internal Termination	Value	Tolerance
L0_CADIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%
L0_CTLIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%
L0_CLKIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%

7.3 DDR SDRAM and Miscellaneous Pins

This section includes electrical specifications for all DDR SDRAM pins described in “DDR SDRAM Memory Interface Pins” on page 47, and the THERMTRIP_L, RESET_L, LDTSTOP_L, PWROK, VID[4:0], TCK, TMS, TRST_L, TDI, TDO, DBREQ_L, and DBRDY pins described in “Miscellaneous Pins” on page 49.

7.3.1 Operating Conditions

Table 17. DC Operating Conditions

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ref}	Reference voltage (for I/O), MEMVREF pin	V	0.49*V_{DDIO_dc} Min	0.5*V_{DDIO_dc}	0.51*V_{DDIO_dc} Max	1, 12
I_l	Input leakage current Any input: $0 \leq V_{IN} \leq V_{DDIO}$ V (All other pins not under test = 0V)	mA	-1		1	
I_{oz}	Output leakage current Any output: $0 \leq V_{OUT} \leq V_{DDIO}$ V	mA	-1		1	
V_{IH}	Input high voltage (logic 1)	V	V_{ref} + 0.15	-	-	2
V_{IL}	Input low voltage (logic 0)	V	-	-	V_{ref} - 0.15	2
V_{OH}	Output high voltage (logic 1) (for VID[4:0])	V	2.0			
	Output high voltage (logic 1) (for all other pins)	V	1.8			
V_{OL}	Output low voltage (logic 0)	V			0.65	
I_{OH}	Output levels -Output high current (V_{OUT}= V_{DDIO}/2)	mA	-25	-28	-33	3
I_{OL}	Output levels - Output low current (V_{OUT}=V_{DDIO}/2)	mA	25	28	32	3
V_{OD}	Differential output voltage (for CK & $\overline{CK}$)	V	1.2	1.3	1.4	4
ΔV_{OD}	Change in V_{OD} magnitude	mV	-100	-	100	5
V_{OCM}	Output common mode voltage (for CK & $\overline{CK}$)	V	1.1	1.25	1.4	6
ΔV_{OCM}	Change in V_{OCM} magnitude	mV	-100	-	100	7

Notes:
The notes for Table 17 through Table 20 appear on page 61.

Table 18. AC Operating Conditions

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ref}	Reference voltage (for I/O), MEMVREF pin	V	V_{ref}(DC) - 2%		V_{ref}(DC) + 2%	1
V_{IH}	Input high voltage (logic 1)	V	V_{ref} + 0.35	-		2
V_{IL}	Input low voltage (logic 0)	V		-	V_{ref} - 0.35	2
V_{OD}	Differential output voltage (for CK & $\overline{CK}$)	V	1.0	1.3	1.6	4
ΔV_{OD}	Change in V_{OD} magnitude	mV	-150	-	150	5
V_{OCM}	Output common mode voltage (for CK & $\overline{CK}$)	V	0.9	1.25	1.6	6
ΔV_{OCM}	Change in V_{OCM} magnitude	mV	-200	-	200	7

Table 19. Input Capacitance

Symbol	Parameters	Unit	Min	Typ	Max	Notes
C_{in}	Input capacitance (DQ & DQS)	pF	3.0	3.5	4.0	
ΔC	Delta Input capacitance	pF	-	-	0.4	8

Table 20. Slew Rate of DDR SDRAM Signals

Symbol	Parameters	Unit	Min	Typ	Max	Notes
S_{OUT}	Output slew rate (pullup and pull-down)	V/ns	3	5	8	9
S_{OUT_Ratio}	Output slew rate ratio between pullup and pulldown		0.75	1	1.25	10
S_{in}	Input slew rate	V/ns	0.5		4	11

Table 21. Slew Rate of RESET_L, LDTSTOP_L, and PWROK

Symbol	Parameters	Unit	Min	Typ	Max	Notes
S_{in}	Input slew rate	V/ns	0.01			13

1. *V_{ref} is expected to be equal to 0.5*V_{DDIO} and to track variations in the DC level of the same. Peak to peak noise on V_{ref} may not exceed $\pm$ 2% of the DC value.*
2. *The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. The receiver effectively switches to the new logic state when receiver input crosses the AC level. The new logic state is maintained as long as the input stays beyond the DC threshold.*
3. *With compensation the granularity between NMOS current and PMOS current cannot exceed 3mA. The range is 6mA due to 10% variation.*
4. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
5. *ΔV_{OD} is the change in magnitude between the differential output voltage while driving a logic 0 and while driving a logic 1.*
6. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage magnitude relative to ground under DC or AC conditions.*
7. *ΔV_{OCM} is the change in magnitude between the output common mode voltage while driving a logic 0 and while driving a logic 1.*
8. *ΔC means the difference in capacitance between any MEMDATA/MEMDQS pin to any other MEMDATA/MEMDQS pin.*
9. *Pullup and pulldown slew rate is measured into R_{TT} (50 Ohms) to V_{TT} as shown in Figure 5. The slew rate is measured between $V_{ref} \pm$ 300 mV. It is designed for any pattern of data, including all outputs switching and only one output switching.*
10. *The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.*
11. *The slew rate is measured at the CPU pin between $V_{ref} \pm$ 150 mV. Minimum and maximum input slew rate specification is set based on DRAM output slew rate specification.*
12. *VDDIO_dc is defined in Table 30 on page 79.*
13. *The slew rate is measured at the CPU pin between $V_{ref} \pm$ 150 mV. Minimum input slew rate specification is based on HyperTransport™ input minimum slew rate specification for single-ended signals.*

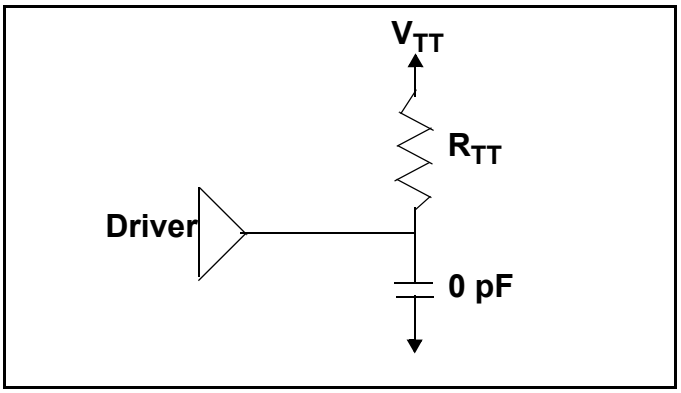


Figure 5. Slew Rate Measurement Example

Table 22. Package Routing Skew

Routing Measurement	Skew (ps)
Any MEMCLK clock pair to any other MEMCLK clock pair	± 100
Any MEMCLK pair to any MEMDQS pair	± 100
Any MEMDQS pair to any MEMDATA associated within pair	± 75
Any MEMCLK pair to any MEMADD/CMD	± 100
Pad skew	± 250

7.3.2 AC Operating Characteristics

Table 23. Electrical AC Timing Characteristics for DDR SDRAM Signals

Symbol	Parameters	Unit	Min	Typ	Max	Notes
tCK	MEMCLK cycle time	ps	5000	-	10000	15
tCH	MEMCLK high pulse width	ps	0.45*tCK	-	0.55*tCK	
tCL	MEMCLK low pulse width	ps	0.45*tCK	-	0.55*tCK	
tCKS	MEMCLK output skew	ps	-350	-	350	1,2,3
tDQSH	MEMDQS high pulse width	ps	0.45*tCK	-	0.55*tCK	1
tDQSL	MEMDQS low pulse width	ps	0.45*tCK	-	0.55*tCK	1
tDQS	MEMCLK to MEMDQS	ps	-350	-	350	1,4,5
tDSS	MEMDQS falling edge to MEMCLK rising edge	ps	0.45*tCK - 350	-	-	1,6,7
tDSH	MEMCLK rising edge to MEMDQS falling edge	ps	0.45*tCK - 350	-	-	1,6,7
tDQSQV	MEMDQS to MEMDATA shift (when data becomes valid)	ps	-{0.5* tDQSHmax - [638]}	-	-{0.5* tDQSHmin + [638]}	1,8,9
tDQSQIV	MEMDQS to MEMDATA shift (when data becomes invalid)	ps	{0.5*tDQSH-min - [638]}	-	{0.5* tDQSHmax + [638]}	1,8,9
t1	MEMADD/CMD to MEMCLK (unbuffered DIMM environment - MEMADD/CMD are launched 3/4 clock early)	ps	- 663	-	663	1,10,11
t3	MEMDATA edge arrival relative to MEMDQS	ps	-{tCK/4 - [350+0.2* (tCK/4)]}	-	tCK/4 - [350+0.2* (tCK/4)]	12,13,14

1. *Write cycle timing parameter.*
2. *The skew consists of pad output skew (± 250ps) and package routing skew between any two clock pairs (± 100ps).*
3. *tCKS timing parameter, refer to Figure 6 on page 65.*
4. *The timing consists of pad output skew (± 250ps) and package routing skew between any MEMCLK to any MEMDQS (± 100ps).*
5. *tDQS timing parameter, refer to Figure 7 on page 65.*
6. *The skew consists of pad output skew (± 250ps) and package routing skew between any MEMCLK to any MEMDQS (± 100ps). Minimum DQS pulse width is 45% of MEMCLK.*
7. *tDSS, tDSH timing parameters, refer to Figure 8 on page 66.*
8. *During write, DQ signals are driven quarter clock earlier such that DQS is placed in the center of data eye window. The skew consists of pad output skew (± 250ps), package routing skew between any DQS signals and it's associated DQ signals (± 75ps) and maximum clock granularity (± 312.5 ps).*

9. tDQSQV and tDQSQIV timing parameters apply only within DQS and its associated DQ signals. Refer to Figure 9 on page 67.
10. The skew consists of pad output skew (± 250 ps) and package routing skew (± 100 ps) between any MEMCLK pair to any MEMADD/CMD signal. Maximum clock granularity skew is 312.5 ps.
11. t1 timing parameter, applies to unbuffered DIMM environment- MEMADD/CMD signals are launched 3/4 clock early. The granularity term is included in this parameter only. Refer to Figure 10 on page 68.
12. Read cycle timing parameter.
13. The PDL placement uncertainty is 20%. Package skew between DQS and its associated DQs is 75ps. The sum of setup/hold time & receiver uncertainty is 275ps.
14. t3 timing parameter, refer to Figure 11 on page 69.
15. The slow operation of 10ns cycle time is specifically included for functional test purpose only. All electrical characterization will be performed at full speed however all functional tests will be performed at 10ns cycle time.

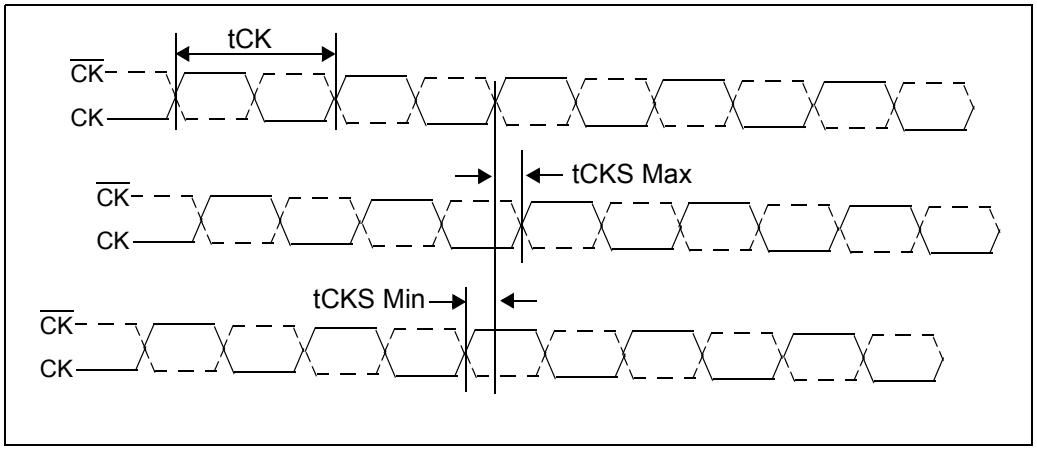


Figure 6. MEMCLK Output Skew

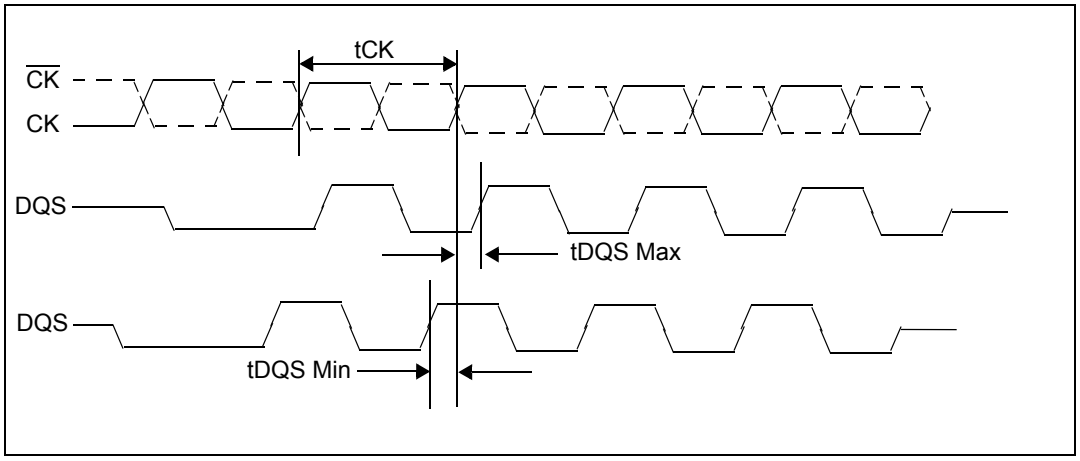


Figure 7. MEMDQS Timing Parameter

t

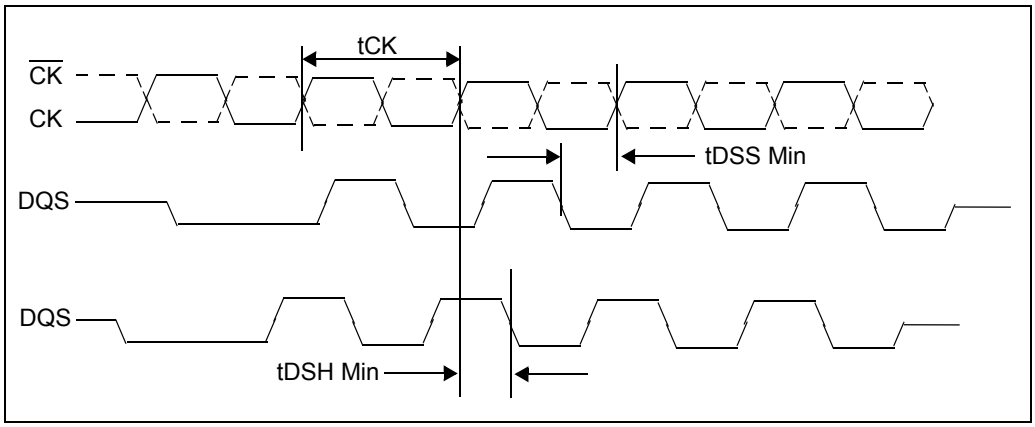


Figure 8. DSS/tDSH Timing Parameters

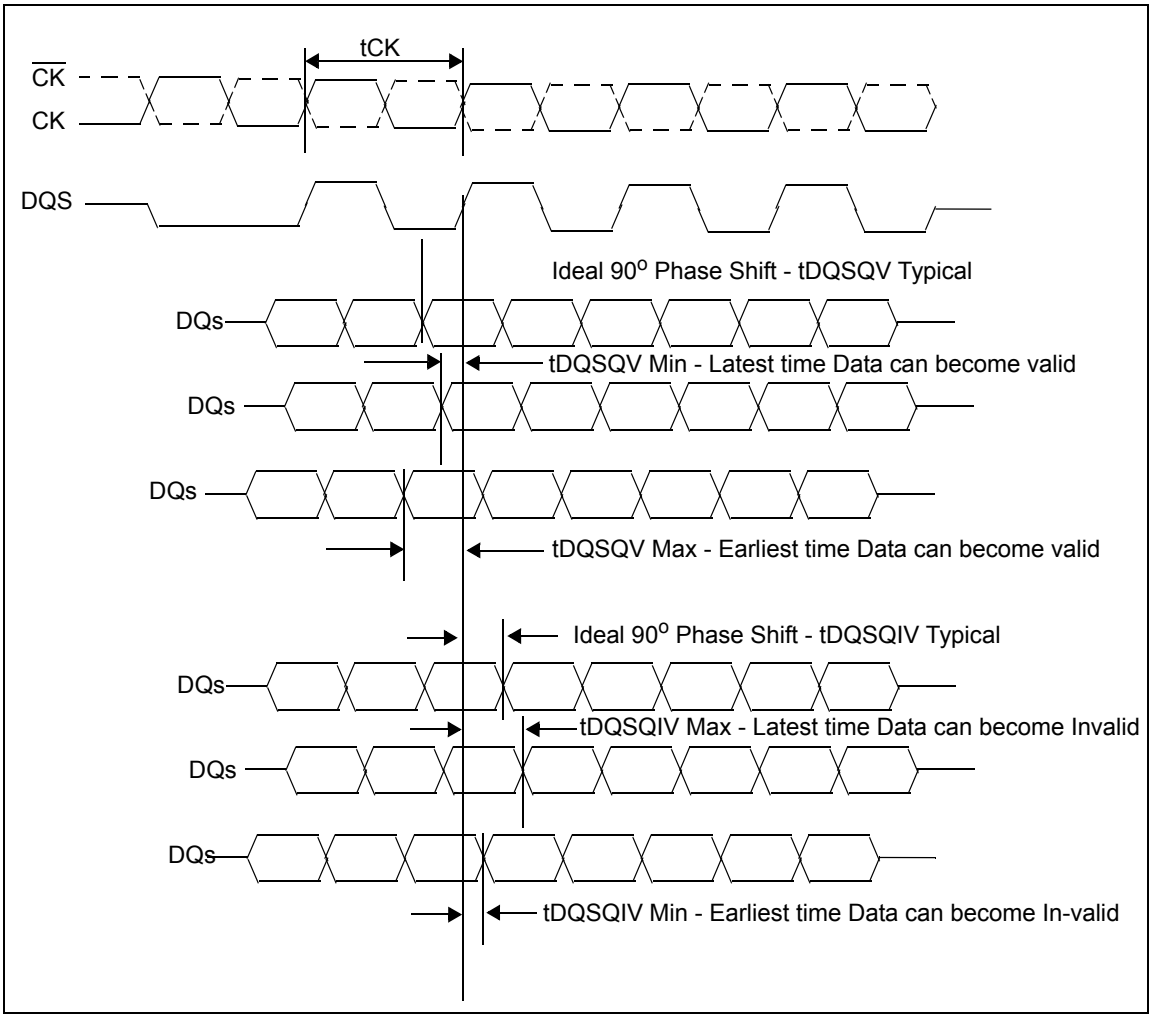


Figure 9. tDQSQV/tDQSQIV Timing Parameters

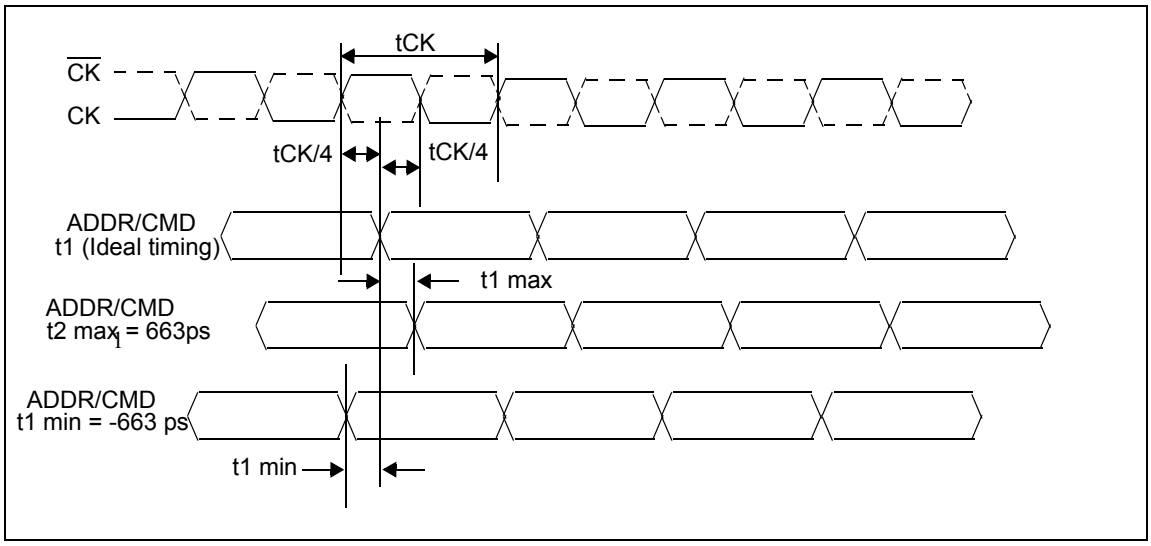


Figure 10. MEMADD/CMD to MEMCLK Timing Parameter

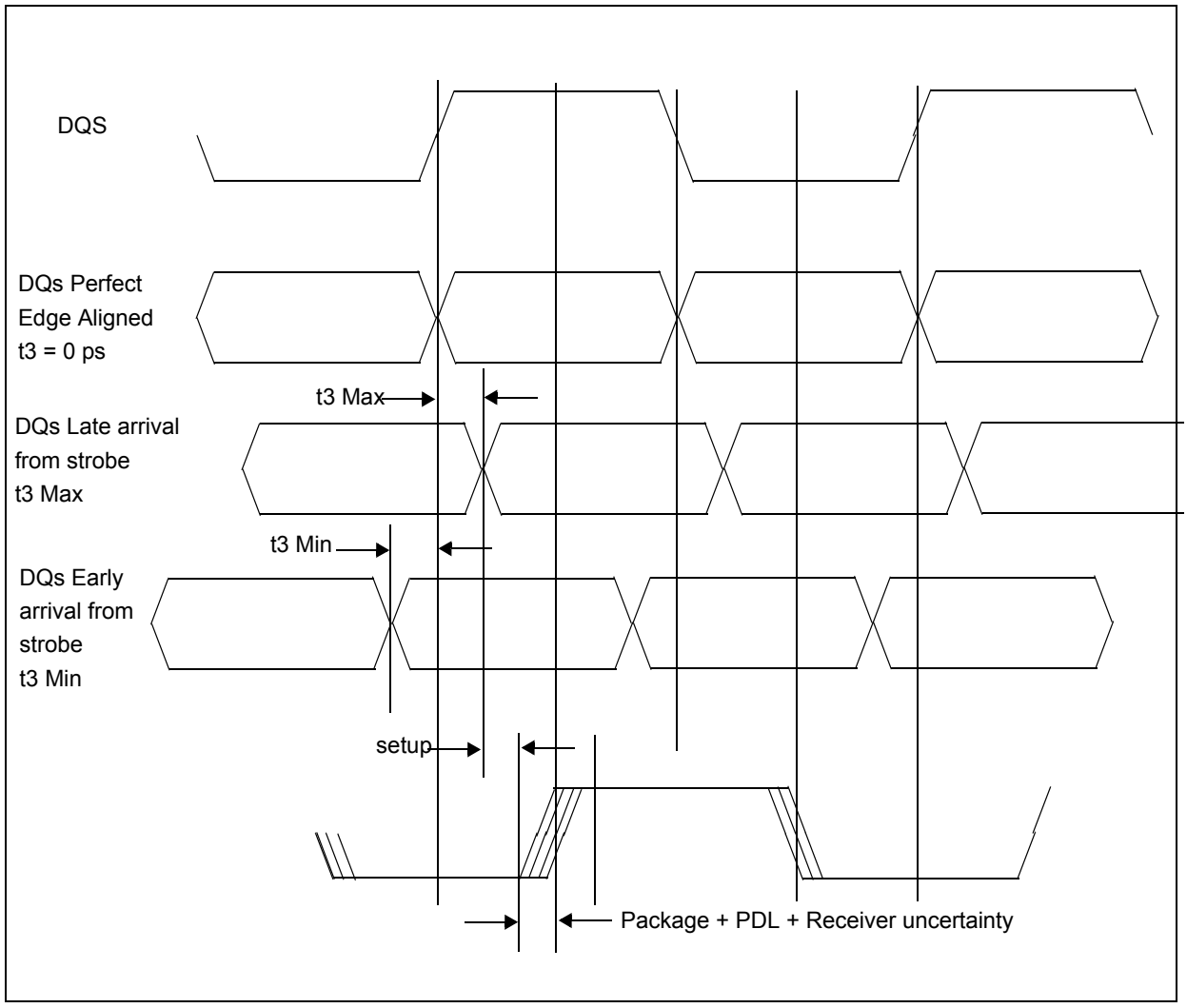


Figure 11. MEMDQS Edge Arrival Relative to DQs

7.4 Clock Pins

7.4.1 Operating Conditions

Table 24. DC Operating Conditions for CLKIN_H/L and FBCLKOUT_H/L Pins

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ID}	Differential Input Voltage	mV	300		2400	
DeltaV_{ID}	Change in V_{ID} Magnitude	mV	–50		50	
V_{ICM}	Input Common Mode Voltage	mV	VTT–100	VTT	VTT+100	
DeltaV_{ICM}	Change in V_{ICM} Magnitude	mV	–50		50	
V_{OD}	Differential Output Voltage	V	1.2	1.3	1.4	1
DeltaV_{OD}	Change in V_{OD} Magnitude	mV	–50		50	2
V_{OCM}	Output Common Mode Voltage	V	1.1	1.25	1.4	3
DeltaV_{OCM}	Change in V_{OCM} Magnitude	mV	–50		50	4

Notes:

1. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
2. *DeltaV_{OD} is the change in magnitude between the differential output voltage while driving logic 0 and while driving logic 1.*
3. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage relative to ground under DC or AC conditions.*
4. *DeltaV_{OCM} is the change in magnitude between the output common mode voltage while driving logic 0 and while driving logic 1 under DC or AC conditions.*

Table 25. AC Operating Conditions for CLKIN_H/L and FBCLKOUT_H/L Pins

Symbol	Parameter	Unit	Min	Typ	Max	Notes
F (PLL mode, VDDA=2.5 V)	Input Frequency Range (SSC)	MHz	198.8		200	6
DC	Input Duty Cycle (CLKIN_H/L)	%	30		70	7
T_{JC}	Jitter, Cycle-to-Cycle	pS	0		200	
V_{BIAS}	Input BIAS Voltage Node	mV	VTT	VTT	VTT	
V_{ID}	Differential Input Voltage	mV	400		2300	
DeltaV_{ID}	Change in V_{ID} Magnitude	mV	–150		150	
V_{ICM}	Input Common Mode Voltage	mV	V_{BIAS}–200		V_{BIAS}+200	
DeltaV_{ICM}	Change in V_{ICM} Magnitude	mV	–200		200	
V_{OD}	Differential Output Voltage	V	1.2	1.3	1.4	1
DeltaV_{OD}	Change in V_{OD} Magnitude	mV	–100		100	2
V_{OCM}	Output Common Mode Voltage	V	1.1	1.25	1.4	3
DeltaV_{OCM}	Change in V_{OCM} Magnitude	mV	–100		100	4
I_F	Input Falling Edge Rate	V/ns	1.2		10	5
I_R	Input Rising Edge Rate	V/ns	1.2		10	5
C_{IN}	Input Capacitance	pF	0		5	

Notes:

1. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
2. *Delta V_{OD} is the change in magnitude between the differential output voltage while driving logic 0 and while driving logic 1.*
3. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage relative to ground under DC or AC conditions.*
4. *Delta V_{OCM} is the change in magnitude between the output common mode voltage while driving logic 0 and while driving logic 1 under DC or AC conditions.*
5. *Measured differentially through the range of VICM – 400 mV to VICM + 400 mV.*
6. *Spread spectrum clocking is limited to –0.5% downspread under normal operation.*
7. *Measured at the differential crossing point. Maximum difference of cycle time between two adjacent cycles.*

7.5 Power-Up Signal Sequencing

Figure 12 on page 74 illustrates the signal sequencing requirements during a cold reset (power-up conditions). The HyperTransport™ link reset sequencing is defined in the *HyperTransport™ I/O Link Specification*.

The following list describes the power-up signal sequencing illustrated in Figure . Note that the numbered items correspond with the numbers in Figure 12.

1. RESET_L must be asserted a minimum of 1 ms prior to the assertion of PWROK, as defined in the *HyperTransport™ I/O Link Specification*. If the JTAG interface is used in a system the TMS pin must be asserted a minimum of 10 nS before PWROK assertion and must be held in the High state a minimum of 10 nS after the assertion of PWROK.
2. CLKIN_H/L must be within specification at the time the VDD power supply begins to ramp.
3. PWROK remains deasserted at least 1 ms after both CLKIN_H/L and all voltages to the processor are within specification for operation. The processor determines if there are devices attached to its HyperTransport™ links 10 µs after the assertion of PWROK.
4. After PWROK assertion the VID[4:0] signals change from the metal mask VID[4:0]***** to the value programmed during device manufacturing. The PLL begins locking to the frequency programmed during device manufacturing 160 µs after PWROK is asserted.
5. LDTSTOP_L must be deasserted a minimum of 1 µs before the deassertion of RESET_L, as defined by the *HyperTransport™ I/O Link Specification*.
6. The RESET_L signal remains asserted a minimum of 1 ms after PWROK assertion, as defined in the *HyperTransport™ I/O Link Specification*. The clocks from the transmitters of all HyperTransport™ devices must be stable before RESET_L is deasserted.
7. The MEMCLK_H/L[7:0] signals are stable after BIOS sets the Memory Clock Ratio Valid (MCR) bit in the DRAM Config Upper register.
8. The MEMCKEA/B signals are asserted.

***** The metal mask VID[4:0] is the value driven on the VID[4:0] lines prior to PWROK assertion. Refer to Table 26 for metal mask VID[4:0] values.

Table 26. Metal Mask VID[4:0] Values

Processor Revision[1]	VID[4:0][2]
CG	0Eh
D0, E	12h

1.Refer to the AMD Athlon™ 64 Processor Power and Thermal Data Sheet, order# 30430, for silicon revision determination.

2.Refer to the BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors, order# 26094, for information on translating VID[4:0] encodings to voltage levels.

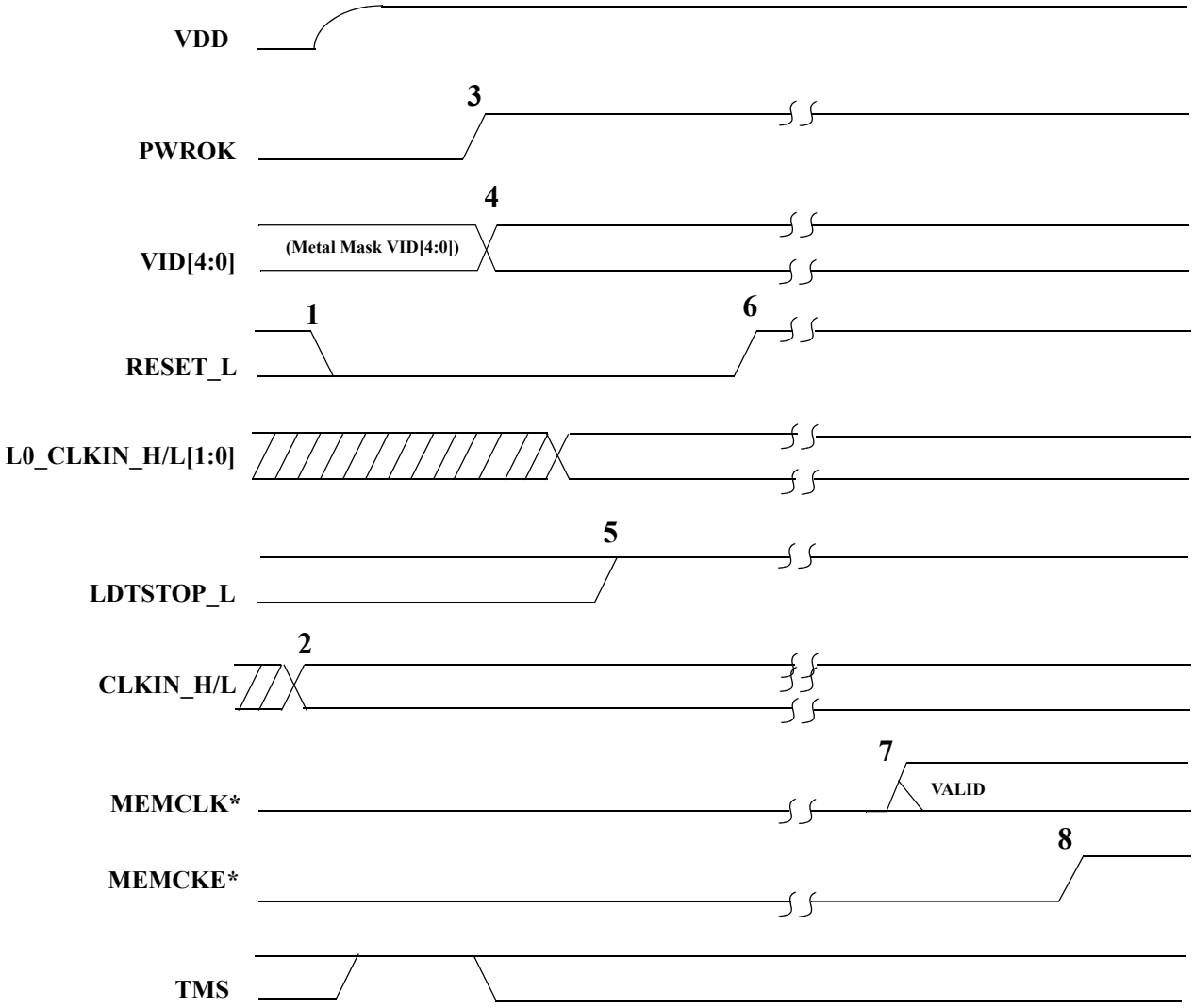


Figure 12. Power-Up Signal Sequencing

7.6 Reference Information

Table 27. Internal Termination for Miscellaneous Pins Interface

Pin	Type[2]	Internal Termination	Value	Tolerance
CLKIN_H/L	I-IOD	None[1]		
FBCLKOUT_H/L	O-IOD	80-ohm differential termination		±50%
RESET_L	I-IOS	None		
PWROK	I-IOS	None		
VID[4:0]	O-IOS	None		
LDTSTOP_L	I-IOS	None		
THERMDA	A	None		
THERMDC	A	None		
THERMTRIP_L	O-IO-OD	None		
COREFB_H/L	A	None		
TCK	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TMS	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TRST_L	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TDI	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TDO	O-IOS	Pullup to VDDIO	533 ohms	±50%
DBREQ_L	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
DBRDY	O-IOS	Pullup to VDDIO	533 ohms	±50%

Notes:

1. *CLKIN_H/L inputs have DC voltage BIAS generating circuits on the inputs. These consist of both a ~250-ohm pullup resistor to VTT on each input and a ~250-ohm series input resistor.*
2. *Refer to "Pin Descriptions" on page 45 for definitions in pin Type column.*
3. *Systems that do not require use of these pins can rely on the internal termination to pull the signals to the proper inactive state. When these pins are used they must not be driven with open-drain outputs or additional termination is required.*

Table 28. External Required Circuits (Pins Not Normally Used in System)

Pin	External Circuit (Non-Operating)[1]
STRAP_HI_E11	Tied to VDDIO_SUS through resistor
STRAP_LO_F11	Tied to VSS through resistor
STRAP_HI_AF12	Tied to VDDIO_RUN through resistor
STRAP_HI_AJ12	Tied to VDDIO_RUN through resistor
STRAP_LO_AH6	Tied to VSS through resistor
STRAP_LO_AG9	Tied to VSS through resistor
STRAP_LO_AF10	Tied to VSS through resistor
STRAP_LO_AJ10	Tied to VSS through resistor
STRAP_LO_Ah10	Tied to VSS through resistor

Notes:

1. See the AMD Athlon™ 64 939 Motherboard Design Guide, order# 30474, for proper resistor values.

7.7 Thermal Diode

An on-die thermal diode is provided as a tool for thermal management. An external sensor is necessary to measure the temperature of the thermal diode.

Thermal solutions should be not designed and validated using the thermal diode. Thermal solutions should be designed and validated against the case temperature specification per the methodology specified in *AMD Athlon™ 64 and AMD Opteron™ Processors Thermal Design Guide, order# 26633*.

7.7.1 Thermal Diode Specifications

Table 29. Thermal Diode Specifications

Symbol	Parameter	Units	Min	Typ	Max	Notes
I	Sourcing Currents	µA	5		500	1
T_{Offset}	Temperature Offset, Rev CG and prior silicon revisions	°C	0		52	2, 3, 4, 5, 7
	Temperature Offset, Rev D0 and later silicon revisions	°C	-31		52	2, 3, 4, 5, 6, 7

Notes:

1. *The sourcing current should always be used in forward bias.*
2. *The temperature offset is used to normalize the thermal diode measurement to reflect case temperature at the worst case conditions for a part.*
3. *This diode offset supports temperature sensors using two sourcing currents only. Single sourcing current implementations are not supported by AMD.*
4. *The temperature offset is unique for each processor and is programmed at the factory. The diode offset value is found in the Thermtrip Status Register described in the BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors, order# 26094.*
5. T_{Offset} *should be subtracted from the temperature sensor reading. If the temperature sensor has an ideality factor different from 1.008, a small correction to this offset is required. Contact your temperature sensor vendor to determine if additional correction is required.*
6. *Negative* T_{Offset} *capability is supported in Rev D0 and later silicon. Refer to the Thermtrip Status Register described in the BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors, order# 26094, for details. Refer to the AMD Athlon™ 64 Processor Power and Thermal Data Sheet, order# 30430, for silicon revision determination.*
7. *Temperature is in degrees Celsius on the* $T_{CONTROL}$ *scale.*

7.7.2 Relationship of T_{CASE} Max and $T_{CONTROL}$ Max

T_{CASE} max is the maximum case temperature specification for a lidded processor. Thermal solutions should be designed to this specification. It is the governing temperature specification for the processor.

T_{CASE} max is a physical temperature specification in degrees Celsius that can be measured at the center of the lid with a thermocouple. The correct method for measuring case temperature is discussed in the *AMD Athlon™ 64 and AMD Opteron™ Processors Thermal Design Guide, order# 26633*. The case temperature specification is provided in the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet,* order# 30430. For Rev D0 and later revisions, the case temperature specification is provided in the THERMTRIP Status Register and is discussed in the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094.

$T_{CONTROL}$ max (maximum control temperature) is a non physical temperature on an arbitrary scale that can be used for system thermal management policies.

$T_{CONTROL}$ = dual sourcing current temperature sensor measurement - T_{OFFSET} (thermal diode temperature offset)

$T_{CONTROL}$ max represents the value at which the processor has reached T_{CASE} max when measuring the thermal diode with a dual sourcing current temperature sensor (see Figure 13). The value for $T_{CONTROL}$ max is provided in the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet,* order# 30430.

$T_{CONTROL}$ max allows the thermal diode to be used to maintain the processor within its case temperature specification. The accuracy of the temperature sensor, typically ±1 C to 5 C, must be considered when setting thermal trip points. System thermal management (e.g. fan control) should be designed to prevent the case temperature from being exceeded even in transient situations. For example if the processor is in an ACPI C1 Halt state with a low fan speed and a high power application is started, the fan speed policy must ensure that the processor never exceeds the $T_{CONTROL}$ max limit. This requires increasing the fan speed before reaching $T_{CONTROL}$ max.

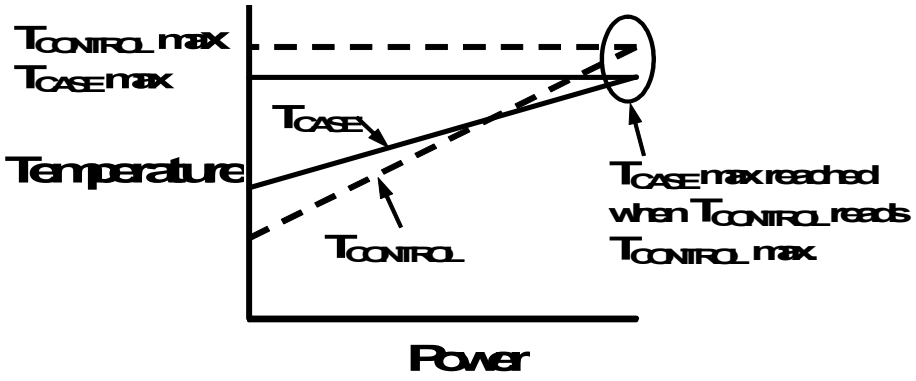


Figure 13. T_{CASE} Max and $T_{CONTROL}$ Max Relationship

7.8 Power Supplies

7.8.1 Operating Conditions

Table 30. Combined AC and DC Operating Conditions for Power Supplies

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VID_VDD	VID requested VDD supply level	V	See Note 10			5
VDD_dc	VDD supply voltage	V	VID_VDD –50 mV	VID_VDD	VID_VDD +50 mV	
VDD_ac	VDD supply voltage	V	VID_VDD –140 mV		VID_VDD +150 mV	11
VDD_PON (Metal Mask VID[4:0])	VDD Supply Voltage before PWROK assertion during power-on, Rev CG	V	1.15	1.20 (0Eh)	VDD_max	7, 12
VDD_PON (Metal Mask VID[4:0])	VDD Supply Voltage before PWROK assertion during power-on, Rev D0 and E	V	1.05	1.10 (12h)	VDD_max	7, 12
VDDIO_dc	VDDIO supply voltage for DDR 333 and below	V	2.40	2.50	2.60	9
VDDIO_dc	VDDIO supply voltage for DDR 400 and below	V	2.50	2.60	2.65	9
VDDIO_ac	VDDIO supply voltage	V	VDDIO_dc -150 mV		VDDIO_dc +150 mV	8
VLDT	VLDT supply voltage	V	1.14	1.20	1.26	
VTT_dc	VTT supply voltage	V	VDDIO_dc Min/2 - 50 mV	VDDIO_dc Typ/2	VDDIO_dc Max/2 + 50 mV	
VTT_ac		V	VTT_dc - 150 mV		VTT_dc + 150 mV	8
VDDA	VDDA supply voltage	V	2.40	2.50	2.60	
IDD	VDD power supply current	A	See Note 10			
IDDIO1	VDDIO power supply current	A		1.9	2.2	3
IDDIO2	VDDIO power supply current in S3 state	mA			480	
ITT1	VTT power supply current	mA			125	1, 4
ITT2	VTT power supply current in S3 state	mA			125	
ILDT	VLDT power supply current	mA			500	
IDDA	VDDA power supply current	mA			33	
IDDslew1	VDD power supply current change during normal operation	A/µs			$.0583 * f^{MHz}$	2, 6

Table 30. Combined AC and DC Operating Conditions for Power Supplies

Symbol	Parameter	Unit	Min	Typ	Max	Notes
IDDslew2	VDD power supply current change upon reset exit	A/µs			270	2
IDDslew3	VDD power supply current change upon stop grant entry	A/µs	–270			2
IDDslew4	VDD power supply current change upon stop grant exit	A/µs			270	2
IDDslew5	VDD power supply current change upon non-reset power failure	A/µs	–4.25			2

1. *VTT must both sink and source current.*
2. *Current slew rates are controlled by ramping up or down the core frequency in steps during these sequences to control in-rush currents.*
3. *VDDIO current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.)*
4. *VTT current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.)*
5. *The processor drives a VID code corresponding to this voltage.*
6. *For example, the IDDslew1 calculation for a 1.2 GHz part is (.0583 x 1200)=69.96 A/µS.*
7. *The processor's VID[4:0] outputs select VID_PON nom before PWROK is asserted. Transients up to VDD_max are allowed.*
8. *VDDIO_ac and VTT_ac parameters are measured +/- 1ns of all data bus bits switching.*
9. *Systems designed to DDR400 power supply parameters will also operate correctly with DDR333 and below.*
10. *Refer to the AMD Athlon™ 64 Processor Power and Thermal Data Sheet, order# 30430, for these specifications.*
11. *Transient duration below VDD_dc min is limited to < 5µs. Transient duration above VDD_dc max is limited to < 10% duty cycle. Test by probing differentially at COREFB_H and COREFB_L with 20MHz scope bandwidth limit. Test conditions are while running AMD's MAXPOWER64 utility using AMD thermal approved production grade heat sinks in normal room ambient conditions.*
12. *Refer to Figure 12 for power up signal sequencing information on Metal Mask VID[4:0].*

7.8.2 Thermal Power

Refer to the *AMD Athlon™ 64 Processor Power and Thermal Data Sheet,* order# 30430, for thermal power specifications.

7.8.3 Power Supply Relationships

7.8.3.1 Sequencing Relationships

Power supply relationships during power-up, power-down, and entry and exit of any power management state must be controlled in order to avoid damage to the device and help ensure proper operation of the device. Figure 14 shows how these relationships are to be maintained and should be specifically ensured by system power generation and distribution schemes. PWROK must be deasserted as VDD decays during power down. VTT and VDDIO are considered SUSPEND planes (on in both S1(RUN) and S3(SUSPEND) states). VDDA, VDD, and VLDT are considered RUN planes and are powered in the S0 and S1 states only. All power supplies should be turned off during the S4 (SUSPEND to DISK) and S5 (SOFT-OFF) states. VDDIO (RUN) is a power rail used for pull-ups on some

processor signals that connect to devices that are powered off during S3, such as THERMTRIP_L.

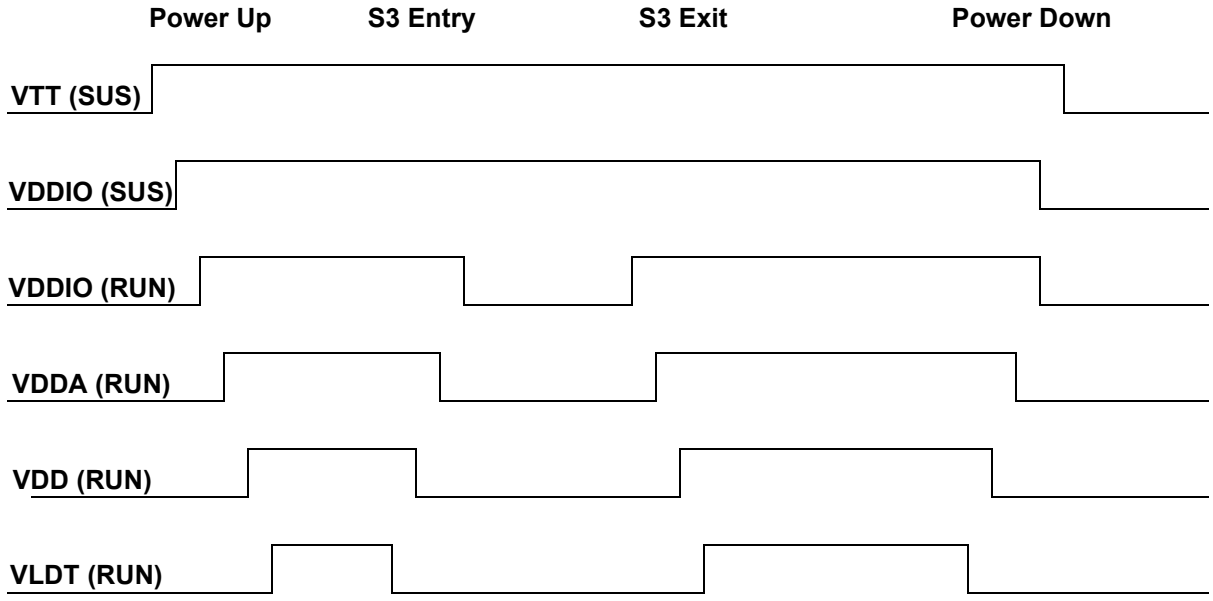


Figure 14. Sequencing Relationships for Power Supplies

Table 31. Sequencing Relationships for Power Supplies

Power Supply Relationship	Unit	Max	Notes
VTT to VDDIO	V	VTT_dc Max	1, 2
VDDIO to VTT	V	VDDIO_dc Max - VTT_dc Typ	1, 3
VDDIO to VDD	V	VDDIO_dc Max	1, 4
VDDA to VDD	V	VDDA Max	1, 5
VDD to VLDT	V	VDD Max	1, 6

Notes:

1. *Sequencing relationships are measured from supply to supply and cover the DC voltage relationships between supplies that must be maintained under all operating conditions including power up, power down, power failure, and power state transitions in order to avoid device or system damage. These relationships can be maintained by propagation of PWRGD signals from one supply rail to the regulator enable of the next supply. The minimum requirements for a proper system implementation are that:*
   - *— VDDIO ramps such that VDDIO/2 <= VTT.*
   - *— VDD ramps such that VDDIO and VDDA are within spec before VDD is enabled.*
   - *— VLDT ramps such that VDD is within spec before VLDT is enabled.*
2. *The VTT to VDDIO relationship allows for VTT to power-up before VDDIO.*
3. *The VDDIO to VTT relationship is critical to avoid overstress of the 2.5-V I/O structures that will occur when VDDIO exceeds VTT by 1.35V during normal operation. VTT must track VDDIO/2 to maintain this specification. During power up and power down VDDIO may exceed VTT by up to 1.5V for no more than 100ms.*
4. *The VDDIO to VDD relationship allows for VDDIO to power-up before VDD.*

5. *The VDDA to VDD relationship allows for VDDA to power-up before VDD. VDDA must power-up before VDD to ensure that internal clock sources are valid before being used and that clock source multiplexors are properly controlled.*
6. *The VDD to VLDT relationship allows for VDD to power-up before VLDT and specifically allows for VDD=VDD_max with VLDT=0 V. VDD must power-up before VLDT to help ensure that PWROK is properly passed from the pins into the VDD power domain such that the deasserted state can be seen in the VLDT power domain.*

7.8.3.2 Sequencing Relationships of Signals to Power Supplies (Stress Conditions)

Once the powerup sequence has been completed and PWROK can be asserted, the sequencing of input signals to the CPU and output signals from the CPU can begin. The requirements from signals to power supplies are summarized by type as follows.

- VDDIO inputs and outputs are allowed to exceed VDDIO by 0.3V and are allowed to be 0.3V below VSS.
- VDDIO inputs are allowed to exceed VTT by VTT_dc Max + 0.3V and are allowed to be 0.3V below VSS.
- VLDT inputs and outputs are allowed to exceed VLDT by 0.3V and are allowed to be 0.3V below VSS.

7.8.3.3 Power Failures

The following conditions must be guaranteed by the motherboard power supply subsystem in the event of a power failure:

- No supply may exceed its maximum specified voltage defined in Table 30.
- VDDIO must not exceed VTT by greater than 1.50V.
- VDDIO may exceed VTT by greater than 1.35V for up to 100ms.

7.8.3.4 Power States

During system power state S3, the RUN supplies (VLDT, VDD, and VDDA) to the CPU are to be turned off. During this operating mode, all internal leakage paths between SUS supplies (VDDIO and VTT) and these powered off planes are disabled. During S0 and S1, all RUN and SUS planes are to be powered on. During S4 and S5, all supplies to the CPU are to be turned off.

8 Package Specifications

8.1 Mechanical Loading for Lidded Parts

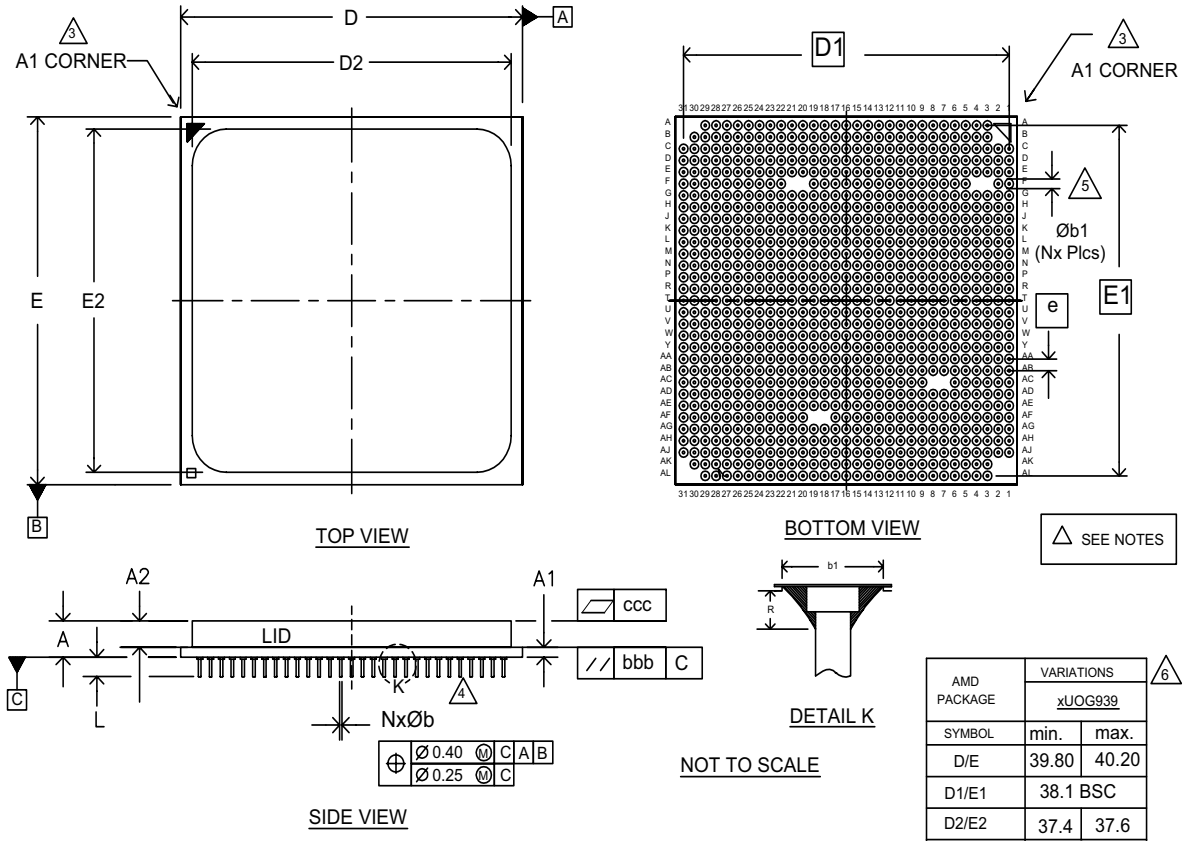
Table 32 provides the mechanical loading specification for lidded parts. These specifications should not be exceeded during heat sink installation, system testing, or system shipment. Refer to the *AMD Athlon™ 64 and AMD Opteron™ Processors Thermal Design Guide, order# 26633*, for more information on properly designing a heat sink to meet these specifications.

Table 32. Mechanical Loading for Lidded Parts

Type	Units	Maximum Force	Notes
Static	lbf	100	1, 2
Dynamic	lbf	200	1, 3

Notes:
1.Load specified for coplanar, uniform contact to lid surface.
2.The static specification specifies the allowable range to be applied by the heat sink to the processor package.
3.The dynamic specification assumes a dynamic load that includes the static load and is applied at 50G for 11ms.

8.2 Package Diagrams

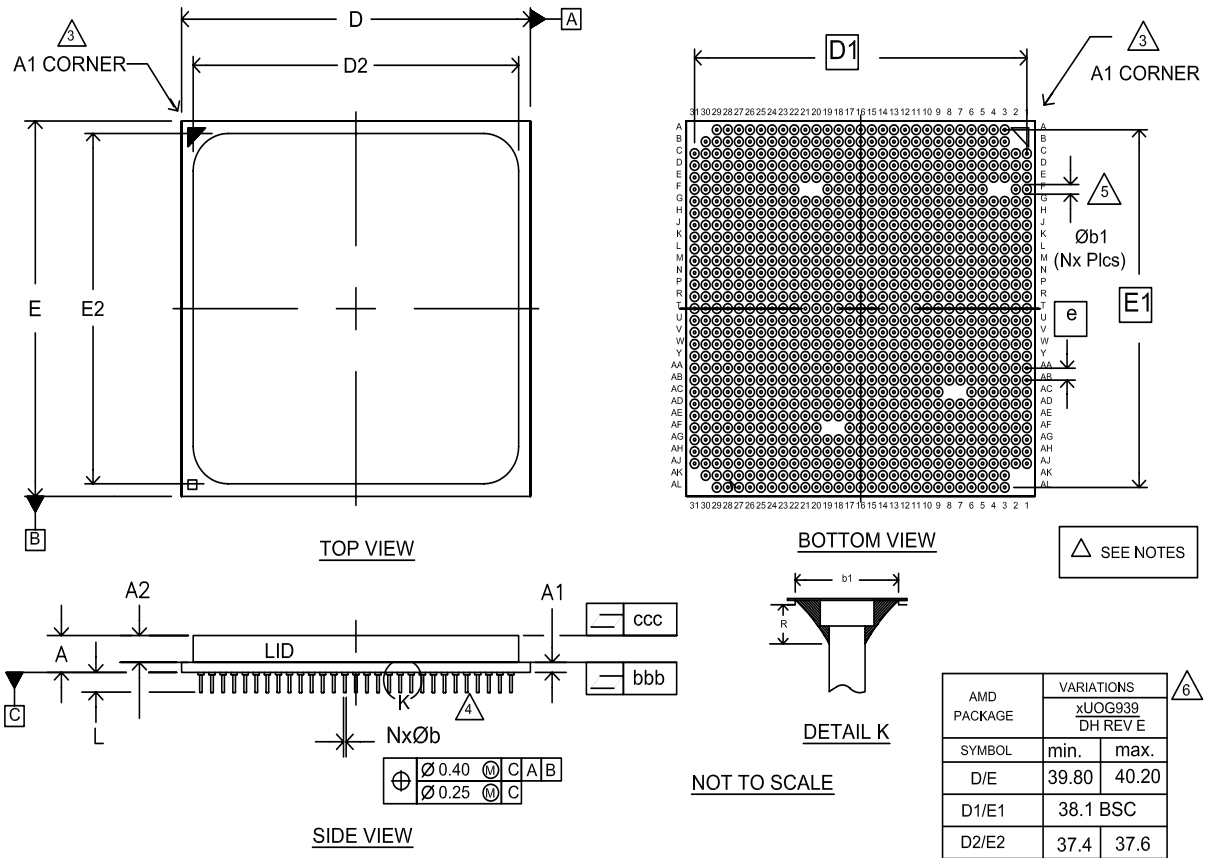


AMD PACKAGE	VARIATIONS xUOG939	
SYMBOL	min.	max.
D/E	39.80	40.20
D1/E1	38.1 BSC	
D2/E2	37.4	37.6
A	4.56 REF	
A1	1.26	1.46
A2	3.05	3.35
e	1.27 BSC	
b	0.275	0.325
b1	0.98	1.08
L	1.95	2.11
M	31	
N	939	
R	0.30 MAX	
bbb	0.10	
ccc	0.125	
WT (gms)	41.0 MAX	

GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner is marked with a triangle on both sides of the package identifies pin A1 corner and can be used for handling and orientation purposes.
4. Pin tips should have radius 0.13.
5. Symbol "M" determines pin matrix size and "N" is number of pins.
6. "x" in front of package variation denotes non-qualified package per AMD 01-002.3.

Figure 15. Organic Micro Pin Grid Array Package: Top, Side, and Bottom Views (Lidded D1)



GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner is marked with a triangle on both sides of the package identifies pin A1 corner and can be used for handling and orientation purposes.
4. Pin tips should have radius 0.13.
5. Symbol "M" determines pin matrix size and "N" is number of pins.
6. "x" in front of package variation denotes non-qualified package per AMD 01-002.3.

AMD PACKAGE	VARIATIONS (6) xUOG939 DH REV E	
SYMBOL	min.	max.
D/E	39.80	40.20
D1/E1	38.1 BSC	
D2/E2	37.4	37.6
A	4.44 REF	
A1	1.14	1.34
A2	3.05	3.35
e	1.27 BSC	
b	0.275	0.325
b1	0.98	1.08
L	1.95	2.11
M	31	
N	939	
R	0.30 MAX	
bbb	0.10	
ccc	0.035	
WT (gms)	39.934 REF	

Figure 16. Organic Micro Pin Grid Array Package: Top, Side, and Bottom Views (Lidded D2)