Implementation of a V.34 modem on a Digital Signal Processor

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Abstract: *The implementation of the modem was mainly done in ANSI C for the 32-bit floating point TMS320C6711™ DSP of Texas Instruments (TI). For the improvement of the execution speed of critical modem subsystems, like the FIR filtering, assembly optimized functions were developed. Although a floating point processor was used for the implementation, the code was written in a 16-bit fixed-point format, so it can be used with fixed-point DSP processors, like the latest TI TMS320C64x family of fixed-point processors.*

1. Introduction

This paper concerns with the V.34 analog modem implementation on a TMS320C6711 DSP [1] at a clock rate of 150MHz. The implementation was financially supported by INTRACOM S.A and is part of a Voice Over IP (VoIP) device, called NetVia™. The selected DSP proved to be an excellent solution for the specific analog modem implementation because of its powerful VLIW DSP-core architecture, flexible peripherals, user-friendly code generation tools (effective ANSI C compiler), and its quite low-cost offer.

The ITU V.34 Recommendation [2] describes a full-duplex modem for Public Switch Telephone Network (PSTN). The modem is operating with selectable symbol rates including the mandatory rates of 2400, 3000, and 3200 symbols/s and the optional rates of 2743, 2800 and 3429 symbols/s and it is based on Quadrature Amplitude Modulation (QAM) modulation and Trellis encoding [3, 4] for all data signalling rates. It achieves data rates up to 33600bps. The channel separation is accomplished with echo cancellation techniques.

2. V.34 transmitter

The V.34 Recommendation explicitly defines the structure of the transmitter, so for a V.34 compliant modem an engineer must follow the Recommendation's specifications. The transmitter consists of the encoder and the QAM modulator.

The V.34 encoder consists of three units that correspond to the stages through which the data flows as it is encoded for transmission. The first of these units, called *parse*, accepts a stream of binary input data, scrambles it, and then partitions these scrambled bits into different groups to be passed to the next unit. The second logical unit, *point-select*, uses the parsed bits to select signal points from a constellation of 2-dimensional (2D) points that has been specified for use in V.34. The third logical unit, *precode*, applies a precoding filter to the signal points to compensate for the noise-enhancement caused by the linear adaptive equalizer in the V.34 receiver. This unit also contains the trellis encoder [3], connected in a feedback configuration, which ensures that the transmitted points correspond to a proper trellis sequence.

The goal of the V.34 encoder is to map binary input data to an output sequence of 2D signal points. These points are modulated using QAM at a specified carrier frequency for transmission over an analog channel. The pulse which is going to be modulated by the carrier signal contains infinite frequency spectrum and so if it is transmitted as it is, intersymbol

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interference (ISI) will be caused. For this reason a lowpass filter (Raised Cosine) is inserted to transform suitably the pulses so as the QAM demodulation is possible without the presence of ISI.

3. V.34 receiver

The structure of the V.34 receiver is not defined by the Recommendation, so it is the designer's responsibility to select a structure and the appropriate algorithms for this structure so as to recover the transmitted data. A telecommunication receiver mainly performs the inverse operations of the corresponding transmitter, but there are additional operations so as to combat the imperfections introduced by the channel, which are amplitude and phase distortion and noise insertion. Due to the fact that a telecommunication receiver is not defined by a recommendation, as in the V.34, the implementation of the receiver is more interesting in terms of research than that of a transmitter one. The V.34 receiver consists of the QAM demodulator and the decoder and the structure that has been implemented is illustrated in figure 1.

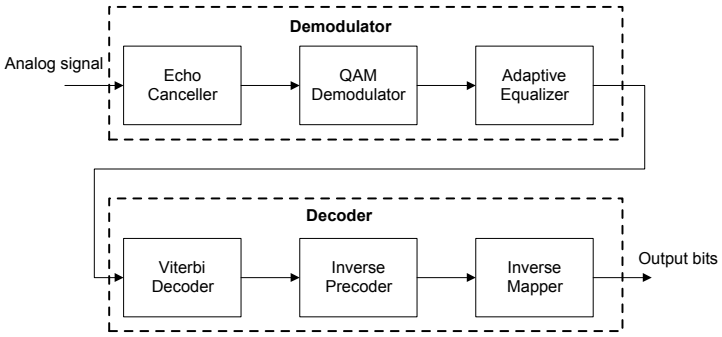

Figure 1 - V.34 receiver diagram.

The echo canceller reduces the amplitudes of the near and far echoes which caused by impedance mismatches in the telephone network. The operation is performed in the passband and for the adaptation of the echo canceller's coefficients the Least Mean Squares (LMS) is used.

The QAM demodulator performs the inverse operation of a QAM modulator. Nevertheless it is a much complex system due to basic reasons: demand for phase recovery of the carrier signal and demand for proper synchronization for the symbol recovery. For the phase correction a Phase Lock Loop (PLL) was implemented with a second order loop filter and a Numerically Controlled Oscillator (NCO), that outputs the corrected carrier frequency [4]. For symbol recovery an interpolation based asynchronous symbol timing using Lagrange polynomial interpolators was implemented. The interpolation filter is a cubic filter which has the Farrow structure. The symbol recovery system has immediate relation to the structure of the adaptive equalizer and this implementation is suitable with the equalizer scheme.

The equalizer corrects the phase and amplitude distortion caused by the communication channel. Its structure was chosen to be a Complex Symbol Spaced Equalizer (CSSE) in baseband, as it is shown in figure 2. The decision device in training mode is a memory containing the training signal TRN and in data mode is the Viterbi decoder. The equalizer's coefficients are adapted by the LMS algorithm.

In figure 3, the real and imaginary error signals are displayed. From the error signals it is found out that the convergence is quite satisfactory and the steady state error is quite small, so the equalizer compensates quite well for the channel distortion.

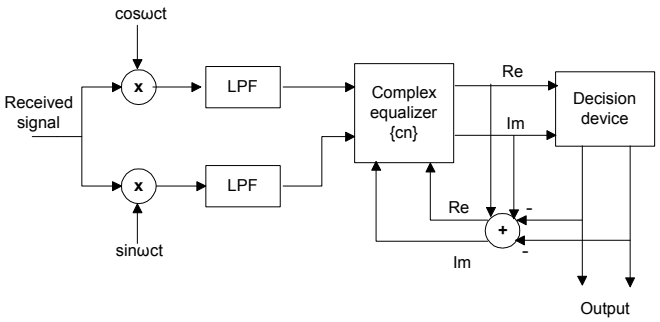

Figure 2 - QAM equalization in baseband.

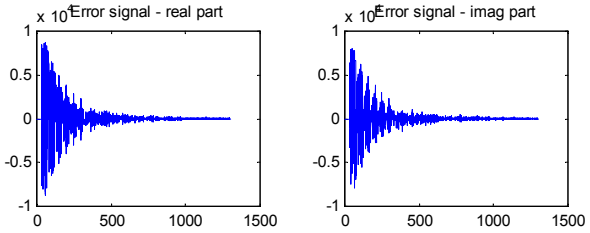

Figure 3 - CSSE baseband equalizer convergence behavior.

The output of the demodulator unit is a sequence of noise-corrupted 2D points. The first step of the decoder unit is to decide to which ideal constellation points these distorted points correspond. This task is accomplished by the *Viterbi decoder*. Next, groups of eight points (i.e., one mapping frame) are passed through the *inverse precoder* and the *inverse mapper* to be decoded into the output data stream.

4. Start-up procedures

V.34 duplex startup consists of four phases. *Phase 1*, the network interaction phase, consists of a 2100 Hz answer tone modulated with a distinctive 15 Hz sine wave with a 20 percent modulation index and a Frequency Shift Keying (FSK) modem at 300bits/s. *Phase 2*, the ranging and probing phase, consists of an initial information exchange ($INFO_0$), ranging and probing sequences, and a second information exchange ($INFO_1$). The information exchanges use 600 bit/s Differential Phase Shift Keying (DPSK) modulation at carrier frequencies of 1200 Hz and 2400 Hz. *Phase 3*, the equalizer and echo canceller half-duplex training phase, consists of a series of signals transmitted first by the answering modem and then by the calling modem and they use QAM modulation with the symbol rate and carrier frequency as they were defined at the end of Phase 2. *Phase 4*, the final duplex training phase, consists of a sequence of scrambled binary 1s and a modulation parameter exchange, following which the selected modulation features and options are enabled. In the references [5, 6], a FSK and a DSPK modem, used in the V.34 start-up procedures, have been studied and implemented.

5. Implementation on the TMS320C6711

The implementation was separated in two main parts: control functionality and digital signal processing functionality. The first part includes the state machines for the start-up procedures. The second part includes all the processing sub-systems, such as: QAM modulator/demodulator (mixers, filtering, phase-locked loop, symbol recovery), LMS

Equalizer (train mode, data mode), encoder (convolutional encoding/precoding), decoder (Viterbi algorithm) and echo-canceller.

In table 1, the 150MHz TMS302C6711™ CPU cycles and the memory requirements for the implementation of the V.34 modem. The CPU cycles which are consumed during the *data* mode, which is the most time consuming mode, are shown. These benchmarks correspond to the following settings of the TMS320C6000 C/C++ compiler (version 4.00): `-o3 -op2 -pmm`. Also these benchmarks assume that the program is stored in an external memory and the data are stored in the internal memory of the processor. From this table it is shown that the real-time requirements are satisfied and also the 7/8 of the processing power of the TMS320C6711 can be used for other purposes (like a G.729 voice codec in a VoIP application) or to implement a multi-channel DSP modem.

Table 1 - CPU cycles and memory requirements.

Symbol rate (symbols/s)	**CPU cycles (*10^6)**	**Time (s)**	**Program memory (K bytes)**	**Data memory (K bytes)**
2400	18.5	0.123	111.9	15.5
3000	19.7	0.131	111.9	15.6
3200	20.3	0.135	111.9	15.6

6. Conclusions

A real-time implementation of a V.34 modem on the TI TMS320C6711 processor has been presented in this paper. This implementation has modest memory requirements and allows the development a single-chip VoIP, as it was the case of the NetVia™ device. Also this modem implementation will be used as an advanced case study or demonstration for the purposes of the lesson *DSP system design* in the 3rd semester of the Master degree course in Electronics, at the Electronics Laboratory. This lesson is currently adapted to include complex applications from field of communications.

7. References

[1] Texas Instruments, *TMS320C62x/C67x Programmer's Guide,* 2000.

[2] ITU-T Rec. V.34, "*A modem operating at data signalling rates of up to 33600 bit/s for use on the general switched telephone network and on leased point-to-point 2-wire telephone-type circuits*", 1998.

[3] L.-F Wei, "*Trellis-Coded Modulation Using Multidimensional Constellations*", IEEE Trans. Info. Theory, vol. IT-33, July 1987, pp. 483-501.

[4] John G. Proakis, Masoud Salehi, "*Communication System Engineering*", Prentice Hall International Editions, 1994.

[5] Michail D. Galanis, Athanassios Papazacharias, Evangelos Zigouris, "*A DSP Course For Real Time Systems Design and Implementation Based On the TMS320C6211 DSK*", 14th International Conference on Digital Signal Processing (DSP2002), Santorini, Hellas (Greece).

[6] Michail D. Galanis, Evangelos Zigouris, "*DSP algorithm implementation on the TMS320C6711 DSK*", Internal report, Electronics Laboratory (ELLAB), Department of Physics, University of Patras, Greece, 2002.
(The report and the code for these implementations are provided at TI University Program's site, http://www.ti.com/sc/docs/general/dsp/programs/shareware/c6000.htm)